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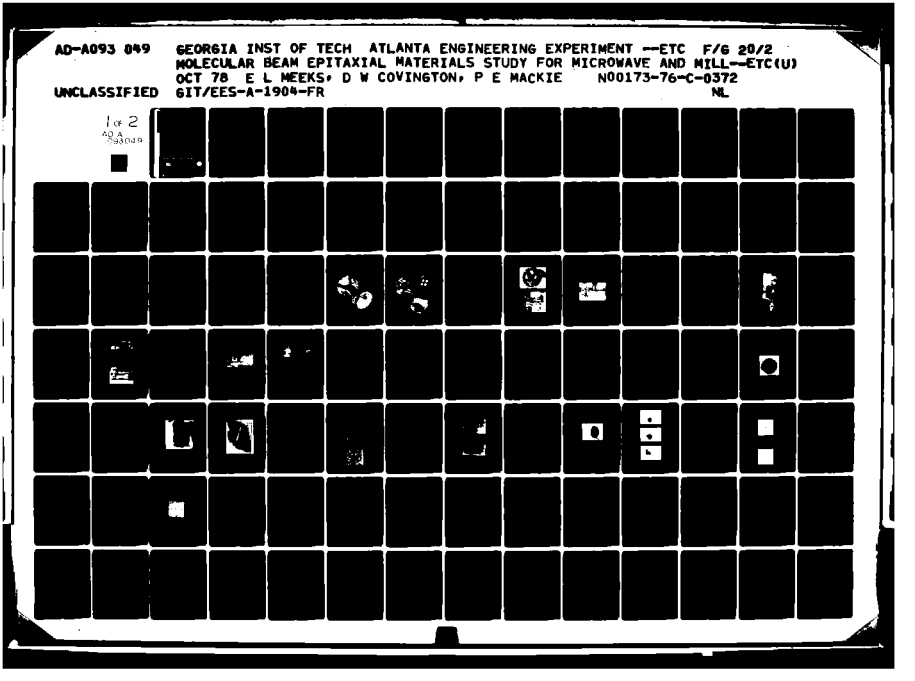

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MOLECULAR BEAM EPITAXIAL MATERIALS STUDY FOR MICROWAVE AND MILLIMETER WAVE DEVICES

By

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Prepared for

NAVAL RESEARCH LABORATORY
WASHINGTON, D. C. 20375

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GEORGIA INSTITUTE OF TECHNOLOGY
Engineering Experiment Station
Atlanta, Georgia 30332

GTEES

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PREFACE

This report describes work performed at the Georgia Institute of Technology Engineering Experiment Station under Contract No. N00173-76-C-0372 during the period 24 September 1976 to 23 October 1978. Funding for the program was provided by Mr. Larry W. Sumney of the Naval Electronics Systems Command with technical administration by Dr. John E. Davey of the Naval Research Laboratory.

SUMMARY

This report described the technical work accomplished in a two year study of molecular beam epitaxial materials for microwave and millimeter wave applications. Analytical techniques including electron diffraction, residual gas analyzer, Auger spectroscopy, electron microprobe, deep level trap spectroscopy, photoluminescence, Schottky barrier diodes, Hall measurements, and X-ray topography were used to relate the deposition conditions to the structural and electrical properties of unintentionally doped layers of GaAs grown by MBE. During the investigation, individual system components were identified which were incompatible with achieving low residual doping levels. Modifications in the system yielded epi-layers with reproducible background doping levels of the order of 10^{14} - 10^{15} cm^{-3}. Two n-type dopants (Sn and Ge) and one p-type dopant (Be) were investigated and used to grow layers for device evaluation. Millimeter wave mixer diodes fabricated from MBE GaAs showed high performance. Layers were also grown for Schottky barrier FETs, Schottky barrier and p^+-n high-low IMPATTs, and p^+-n hyperabrupt varactors, and the static characteristics of these devices were investigated. Barrier heights for Au, Al, and Ag Schottky diodes, on freshly grown layers were lower than barrier heights measured for diodes formed on oxidized GaAs layers. Epilayers of GaAs were also grown on (111) Ge substrates and surface characterizations made for evaluation of crystalline perfection. MBE layers were delivered to the Naval Research Laboratory for photoluminescence analysis, deep level trap measurements, device studies, and MOS surface state characterization.

1: to the 14th power to 10 to the 15th power/cu cm

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1.0 INTRODUCTION

1.1 OVERVIEW

Recent advances in the performance of microwave and millimeter wave solid state devices have in many cases resulted from the utilization of more sophisticated semiconductor materials. To extend device performance toward even higher frequencies requires stringent material characteristics and sophisticated doping profiles which stress the limits of semiconductor growth available with the existing chemical vapor deposition and liquid phase epitaxy techniques. Molecular beam epitaxy (MBE) is an alternative deposition technique that has recently achieved significant success in the preparation of complex structures of III-V, IV-VI and II-VI compounds. Characteristics of MBE that are particularly favorable for device fabrication include atomically smooth surface topography, precise control of growth rates, the introduction of doping or chemical compound species on a monatomic scale during growth, and the ability to achieve electrical isolation between active devices which may find application in monolithic microwave integrated circuits. The objective of the work on this program is to obtain a fundamental understanding of the unique features of MBE which can be exploited to grow precisely controlled, epitaxial material for microwave devices extending into the millimeter range. Areas which are receiving particular emphasis in the present research are the analysis of the crystalline perfection and electrical properties of GaAs layers containing no intentional doping as well as n, n^+, p, and p^+ dopants, a study of Schottky barriers prepared in situ using MBE material, an experimental investigation of millimeter IMPATT devices with precisely tailored doping profiles, and the fabrication and testing of GaAs MESFET's grown upon semi-insulating buffer layers.

1.2 HISTORICAL BACKGROUND

Epitaxial semiconductor growth by MBE involves the condensation of beams of atoms or molecules upon a single crystal substrate. The beams are generated from individually heated, cylindrical effusion cells containing the component elements and doping species. Abrupt changes in the composition and doping of the deposit are derived by the selective shutter modulation of beams projected toward the substrate. Since typical growth rates are of the order of one $\mu m\ hr^{-1}$, this modulation allows very thin layers to be prepared with high precision. The growth process is generally carried out under ultra high vacuum (UHV) conditions at relatively low substrate temperatures. The low substrate temperature minimizes undesirable thermal diffusion effects, and the UHV environment facilitates analytical surface characterizations such as Auger and high energy reflection electron diffraction (RED).

The operating conditions, procedures, and equipment for producing single crystal films of the elemental semiconductors have been established for several years[1-4]. Stoichiometric films of III-V compound semiconductors were more difficult to prepare because the partial vapor pressures of the group V elements are considerably higher than the group III elements at the temperatures needed for practical growth rates. This problem was addressed by Günther[5] who evaporated each component of the compound from separate ovens. The temperature of the substrate was adjusted for the adsorption of the vapor atoms and the subsequent combination of the adatoms into a stable compound. Subsequent advances in growth technique extended the Günther approach and laid the foundations for the further development of MBE.

Using Ge and GaAs substrates that were cleaned in situ with low energy argon ions[6], Davey and Pankey grew epitaxial layers of GaAs with separate ovens

loaded with Ga and As[7]. Arthur's experimental measurements of the equilibrium vapor pressure data for GaAs[8] and his analysis of the interaction between the incident Ga and As species on a heated GaAs surface showed that stoichiometric growth could be realized over a range of substrate temperatures where the ratio of the As_2 to Ga flux was greater than one[9]. High energy electron diffraction analyses by scientists at Bell Laboratories[10,11] and IBM[12-14] further identified the growth conditions for gallium and arsenic stabilized surfaces. This had important implications in understanding the behavior of amphoteric dopants in GaAs[15].

A wide range of dopants for GaAs grown by MBE have been systematically studied by Cho and others. Useful n-type dopants include Sn, Si, and Ge[12,15-19]. For p-type layers, Ge, Mg, Mn, and Be have been employed[12,15,16,19-23]. Other p-type dopants such as Zn may be used when introduced as ionized molecular beams to improve the low sticking coefficients[24].

The results of these investigations have accelerated the applications MBE is finding in active device construction. A. Y. Cho at Bell Laboratories has been particularly active in demonstrating device applications using MBE material. The technology has matured to the extent that critical evaluations can be made of GaAs devices fabricated from MBE layers.

Both Schottky barrier and p-n junction diodes have been constructed which show reverse breakdown voltages that correspond closely to the theoretical values expected for doping levels obtained in these diodes[17]. The quality factors for a lightly doped Schottky diode and the p-n junction diodes were 1.08 and 1.8, respectively, which compare to the value of 1.0 for ideal diodes.

The flexibility of MBE in controlling doping profiles has been demonstrated with hyperabrupt Schottky barrier microwave varactors[25]. These

devices require doping concentrations n that are proportional to a power variation of the distance x measured from the barrier ($n \alpha x^m$). Using a doping profile with m = -1.5 for $0 \leq x \leq 0.4$ micron yielded a diode with a measured capacitance range which varied by a factor of nine over a two volt bias range. This implies a capability for tuning over a three to one bandwidth ratio.

The accurate doping control of MBE has been further established with the successful formation of an IMPATT device using a low-high-low doping profile[26]. A highly doped n^+ layer ($\sim 10^{17}$ cm^{-3}) less than 0.3 μm in width was positioned in the avalanche zone approximately 0.3 μm from a metal Schottky barrier. Doping for the drift region (~ 3.8 μm wide) was 10^{16} cm^{-3}. A noise measurement of 44 dB was reported at an operating frequency of 11.7 GHz, r.f. power of 2.8 watts and an efficienty of 18 percent. No attempt was made to optimize this structure, and it represents a very preliminary result.

Other microwave devices prepared recently with MBE material include mixer diodes[27,28] and FET's[29-31]. Planar Schottky barrier mixer diodes showed quality factors of 1.1 to 1.3, forward series resistances of 4.0 to 8.0 ohms and parasitic capacitances of 0.02 pF[27]. When tested in a double-balanced downconverter, a conversion loss of 5.3 dB was measured at 51.5 GHz. Other Schottky barrier diodes formed with slightly thinner MBE layers (thickness ~ 0.1 to 0.2 μm) and slightly lower donor concentrations (3×10^{16} cm^{-3}) achieved a noise temperature of 55 °K while operating at a frequency of 100 GHz[28].

GaAs metal semiconductor field effect transistors prepared by MBE are also attaining significant performance levels[29-31]. The best noise figures reported for low noise devices with 1.0 μm gate lengths are 3.3 dB (5.6 dB gain) at 10 GHz[30] and 1.9 dB (11.0 dB gain) at 6.0 GHz[31]. Power FET's with

3.0 mm gate widths delivered a 1.0 dB compression power of 1.3 W at 4.4 GHz with a gain of 10 dB and a power added efficiency of 35 percent[31]. Comparative noise figures at 4.0 GHz for FET's constructed with MBE and CVD layers indicated values of 1.4 dB and 0.9 dB, respectively[32].

Initial experiments have also been conducted which demonstrate a planar technology potential for GaAs grown by MBE. By depositing a selective oxide layer, semi-insulating polycrystalline GaAs was grown on the oxide and monocrystalline GaAs was grown in the oxide-free windows for active devices[27] or ohmic contacts[33]. Cho reported that the epi-material deposited in window areas could be doped to 10^{18} cm^{-3} while maintaining a semi-insulating deposit on the oxide[34]. The results of the Zn doping experiments led to the suggestion that two dimensional patterns of doped areas may be written during MBE by scanning ionized doping beams across the growing layer[35].

While the above review traces the development and application of MBE in areas that are directly related to microwave devices, MBE has also offered some exciting possibilities in multilayer $Al_xGa_{1-x}As/GaAs$ optical devices such as double heterostructure lasers[36,37], distributed feedback lasers[38], optical waveguides[39], and dielectric stack interference filters[40-42]. The high degree of layer thickness and composition control afforded by MBE is probably best exemplified by the quantum mechanical phenomena that have been observed in superlattices of $Al_xGa_{1-x}As/GaAs$[43,44]. While multilayers that showed structural periodicities as small as 75 to 110 Å have been formed by chemical vapor deposition[45-47], MBE material has demonstrated a variety of superlattice quantization effects including negative resistance[48], conductance oscillation derived from high field domains[49], shift in the optical band edge[50], direct optical absorption[51], and laser oscillation[52].

1.3 PROGRAM GOALS

The objective of this materials research is to investigate the physical and electrical properties of thin semiconductor layers grown by molecular beam epitaxy which would control the performance of microwave devices extending into the millimeter range. The potential value of MBE for these applications will be further assessed by fabricating and evaluating test devices including IMPATT's and FET's. A basic outline of the program of study is given below.

Phase I. Study of materials problems associated with microwave devices extending into the millimeter range.

Task 1. Study of crystal perfection of thin MBE layers grown on semi-insulating GaAs substrates.

Task 2. Metal-semiconductor interface studies for Schottky barriers on GaAs formed in situ.

Task 3. Preparation and evaluation of n, n^+, p and p^+ layers on GaAs.

Phase II. Evaluation of MBE for microwave devices.

Task 1. Experimental correlation of the performance of millimeter IMPATT devices with the various types of precisely controlled and positioned impurity profiles.

Task 2. The fabrication and performance evaluation of GaAs FET with Schottky barrier gates and semi-insulating buffer layers.

Task 3. The preparation of GaAs FET and IMPATT materials to be delivered to Navy for evaluation.

1.4 DESCRIPTION OF SECTIONS TO FOLLOW

The work described in this report is a basic study of molecular beam epitaxial materials for microwave and millimeter wave device applications. The growth of GaAs by MBE and the general system details are covered in Section 2.0. The fundamental growth processes of MBE are reviewed in Section 2.1. Section 2.2 describes the system assembled at Georgia Tech for growing multilayer devices. The operational procedures including the X-ray and Auger analyses which characterize the substrate prior to deposition are detailed in Section 2.3. Actual deposition parameters employed for growing GaAs are listed in Section 2.4.

In order to understand the basic performance capabilities and limitations of active devices constructed with MBE materials, accurate measurements of a number of material parameters are required. Analytical techniques which measure the crystalline perfection and electrical properties of MBE layers are described in Section 3.0. As indicated in Section 3.1, epitaxial growth conditions are established with the electron diffraction unit installed directly in the MBE system. Hall measurements (Section 3.2) and Schottky barrier diode measurements (Section 3.3) are used to evaluate the electrical properties of the epilayers such as carrier mobility, dopant activation energies, and concentration profiles. Devices such as microwave mixers, FET's and IMPATT diodes are sensitive to the presence of majority carrier traps that degrade high field performance, introduce noisy generation-recombination centers and increase the device sensitivity to light and operating parameter drift[53,54]. The identification of deep level traps described in Section 3.4 provides fundamental information on growth conditions leading to improved material properties[55]. Specimens grown by MBE were also studied

using high resolution photoluminescence techniques (Section 3.5).

Section 4.0 presents the results of a thorough investigation of the unintentional background doping levels for GaAs epilayers grown by MBE. This study developed by correlating the material properties with the deposition parameters monitored during growth. The practical difficulties encountered and the methodologies available for studying background doping concentrations in GaAs are reviewed in Section 4.1. Two unintentional n-type dopants and two unintentional p-type dopants were identified. The characteristics of these dopants are described in Sections 4.2 and 4.3. Under ideal conditions layers are grown with an acceptor dopant background at the 10^{14} to 10^{15} cm^{-3} level. A state-of-the-art assessment in Section 4.4 compares the present data with the deposition parameters and electrical properties of GaAs grown by other laboratories actively involved in MBE.

The properties of MBE GaAs containing intentional doping levels spanning the range 10^{15} to 10^{18} cm^{-3} are given in Section 5.0. As Section 5.2 indicates, a simple relationship exists between dopant oven temperature, doping level, and growth rate for a number of common dopants. The electrical characterization of n-type layers doped with Sn and Ge and p-type layers doped with Be are presented in Section 5.3.

Section 6.0 deals with a basic investigation of metal semiconductor interfaces. A simple modification to the basic MBE system facilitated in situ depositions of Schottky metallizations on freshly grown and oxidized GaAs surfaces (Section 6.2). The results of barrier height measurements for Au, Ag, and Al Schottky diodes are discussed in Section 6.4.

A number of devices were fabricated to further test the microwave and millimeter wave applications of MBE GaAs. The noise figures reported

in Section 7.1 for MBE mixer diodes at 35 GHz compare favorably with noise figures of commercially available diodes. The static characteristics of FETs (Section 7.2) and hyperabrupt varactors (Section 7.4) show potential for good r.f. performance. Schottky barrier and p^+-n high low IMPATT materials have also been grown using MBE (Section 7.3).

Gallium arsenide epilayers were grown on Ge substrates as part of a study of peeled film MBE layers. The preliminary results given in Section 8.0 emphasize techniques for substrate preparation and electron diffraction studies of both the Ge substrate and the GaAs epilayers.

1.5 PRINCIPAL RESULTS

During this two year program, the following results were obtained:

(1) Unintentional acceptor and donor impurities at levels of 10^{15} to 10^{17} cm^{-3} can be introduced in GaAs layers grown in MBE systems containing stainless steel (pp. 95 - 105), beryllia (pp. 82 - 91), and fused quartz (pp. 91 - 95) structural components operating at elevated temperatures. Tantalum (pp. 22, 28) and molybdenum (pp. 28) are presently the preferred materials in MBE system construction.

(2) In contrast to vapor phase epi-GaAs, a residual acceptor in the low 10^{14} cm^{-3} range is commonly observed for unintentionally doped MBE GaAs grown under As-stabilized conditions (p. 104). Photoluminescence and Hall data suggest that this acceptor is either a defect complex and/or carbon with an activation energy of approximately 0.027 eV (p. 103).

(3) Good mobilities were measured for MBE GaAs layers intentionally doped with Sn, Ge, and Be over the concentration range of 10^{15} to 10^{19} cm^{-3} (p. 111). Comparisons between incorporated doping levels for these three elements and the incident beam flux computed from vapor pressure tables indicate that the level of doping can be controlled by measuring the oven temperature (p. 108). These results also show that the sticking coefficients are approximately

unity for GaAs substrate temperatures of 560 to 600 °C.

(4) The precise thickness and doping control characteristic of MBE GaAs yielded high performance millimeter wave mixer diodes (noise figures of 4.85 and 8.3 dB at 35 and 92 GHz, respectively, pp. 130 -138). Static characteristics of Schottky barrier FETs (pp. 138 - 145), p^+-n high-low IMPATTs (pp. 145 - 149), and p^+-n hyperabrupt varactors (pp. 149 -153) also demonstrate the doping profile control required for microwave and millimeter wave devices.

(5) The growth of multilayer, single-crystal GaAs layers on Ge substrates shows potential for the peeled-film device technology (pp. 157 - 159).

(6) Aluminum, gold, and silver Schottky metallizations deposited *in situ* on freshly grown n-type GaAs layers exhibit barrier heights that are approximately 0.10 eV lower than similar barriers formed on GaAs surfaces exposed to ambient oxidation (pp. 124 - 128).

(7) Beams of As_4 molecules generated in conventional MBE systems are not convenient for maintaining the stoichiometry of GaAs surfaces in the 800 °C range that is often employed for annealing ion implanted specimens (pp. 165 - 167).

2.0 GROWTH OF GaAs BY MBE

2.1 GROWTH PROCESS

In thermal evaporation type epitaxial systems, solid materials are vaporized in a controlled vacuum environment by maintaining the material at an elevated temperature. Under suitable conditions, epitaxial films can be formed by condensing the vapor upon a heated substrate. The operating conditions, procedures and equipment for producing single crystal films of the elemental semiconductors using this technique are well known and established[1-4].

The number of molecules N evaporated per unit area per second for a saturated vapor can be written as

$$N = Cp^{*} (MT)^{-1/2} \qquad (1)$$

where

C = constant,

p^{*} = equilibrium vapor pressure (Torr),

M = molecular weight of the vapor constituents, and

T = temperature (°K).

The actual condensation of the vapor at the substrate is a function of the directivity of the source emission, the geometric shape factor describing the fraction of the emission which is actually intercepted by the substrate, and the condensation coefficient.

The structure and properties of semiconductor films are particularly sensitive to the quality of the vacuum environment. High vacuum conditions ($\leq 10^{-9}$ Torr) are desirable to reduce scattering collisions between the emitted particles and residual gases in the system. Another benefit of high vacuum operation is the greatly reduced possibility of sorption of impinging

gas molecules during film growth. Adequate pumping capacity must be provided to minimize the time spent in pumping down the system.

The oven temperatures must be carefully regulated if reproducible growth rates are to be obtained. Other important deposition parameters which are controlled include the substrate temperature, the vacuum quality, and outgassing from the system hardware. Representative deposition rates for thermally evaporated semiconductor films fall into the range of 0.003 to 10.0 μm/hr.

If the thermal evaporation of multi-component alloys or compounds is attempted by simply placing the source material in a single crucible or oven, unbalanced constituent emission rates will often be observed, because constituent vapor pressures will generally differ[56]. This leads to nonstoichiometric film growth. The multi-oven arrangement employed in the molecular beam epitaxy (MBE) system, however, allows the emission rate of each component to be adjusted individually[57]. The equilibrium emission from each oven can be estimated using an expression similar to Equation 1. Adsorption of the emitted species on a heated substrate under suitable reactive conditions results in the formation of a stable compound. The multi-oven configuration provides considerable flexibility not only in altering the composition of the deposited film, but also in selectively introducing precisely defined doped layers while minimizing thermal diffusion of the dopant.

The system requirements for molecular beam epitaxy are basically similar to conventional thermal evaporation systems. The primary components are schematically indicated in Figure 1. Temperatures of the ovens and the substrate are monitored closely. Base pressures less than 4×10^{-9} Torr are typical before the deposition is initiated, but during growth the system

pressure is determined by the As source temperature. Because the deposition occurs under ultrahigh vacuum conditions, it is quite feasible to conduct analyses of the surface structure using electron diffraction techniques[10].

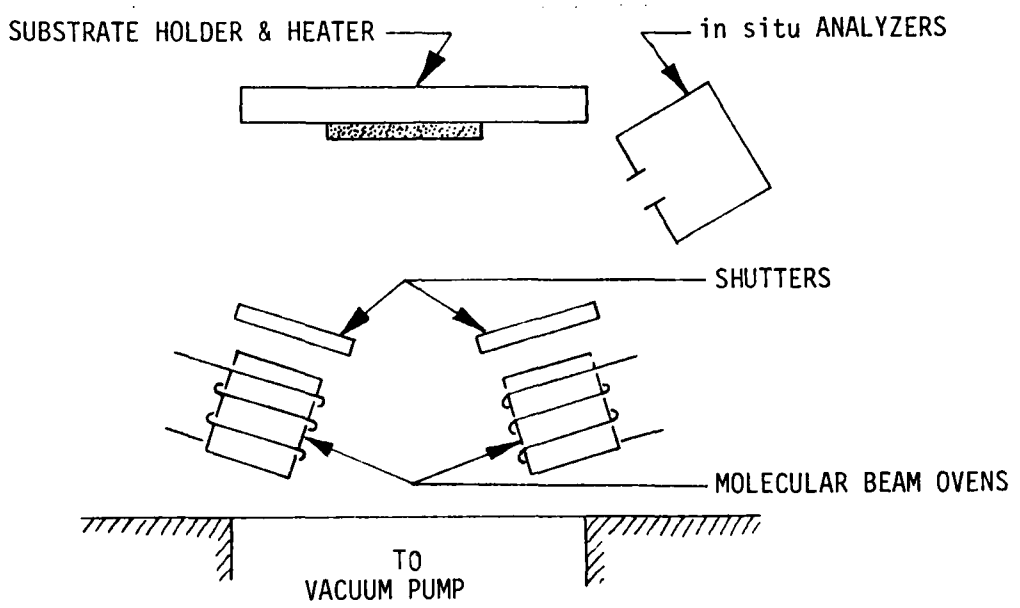


Fig. 1. Molecular Beam Epitaxy System

Chemical contaminants of approximately 0.01 monolayers can be detected with in situ Auger equipment[21]. Mass spectrometers are helpful in regulating the emission during non-equilibrium operation of the molecular beam sources, as well as identifying the partial pressures of residual gases evolved during system pump-down and film deposition[12].

As in any epitaxial system, MBE has certain characteristic features which directly influence its technological applicability in supplying active

material for microwave semiconductor devices. Basic process variables are detailed below which provide additional insight into MBE techniques employed in growing and doping GaAs.

2.1.1 Process Variables

Equation (1) indicates that the number of molecules emitted by a Knudsen cell in equilibrium is proportional to $p^*(MT)^{-1/2}$. Thus the cell temperature and the constituent vaporization pressures of the source material establish the emission flux rate of molecular beam sources. In a typical mutli-oven arrangement for growing doped GaAs layers, one oven is loaded with polycrystalline GaAs to supply As_2 vapor. Another oven contains pure Ga, and a third oven contains the dopant[17]. In a variant loading procedure, pure arsenic is substituted for the polycrystalline GaAs to obtain low background dopings[25]. Representative temperatures for the GaAs and Ga ovens fall in the range of 927 °C and substrates are often heated to 547-577 °C[17,43]. An oven loaded with As typically operates at temperatures of 295 to 347 °C[7,30].

The actual growth rate observed is influenced by the arrival rates of particles effusing from the ovens, the coefficient of condensation, and the lifetimes of the adsorbed particles at the heated substrate. Under conditions of arsenic-stabilized growth, the sticking coefficient for the Ga flux incident upon a GaAs substrate heated to temperatures between 500 and 600 °C is essentially unity. Thus the growth rate R ($\mu m\ hr^{-1}$) for GaAs is determined primarily by the Ga flux[11]. Using the formulation for a Knudsen cell, the following relationship is obtained between R, p^* and T:

$$R = 6.84\ 10^6\ s^2(h^2+s^2)^{-1}\ p^*\ T^{-1/2} \qquad (2)$$

where s = radius of oven aperture and

h = oven to substrate spacing.

The Ga flux in molecules cm^{-2} sec^{-1} is written as

$$F_{Ga} = 4.21\ 10^{21}\ s^2(h^2+s^2)^{-1}\ p^*T^{-1/2} \qquad (3)$$

A regression analysis of vapor pressure data[56] for Ga and As allows the vapor pressure to be expressed directly in terms of the oven temperature

$$\log p^* = B - AT^{-1} \qquad (4)$$

where A = 14613.5 and B = 8.3814 for Ga. The As oven temperature is typically adjusted for an As_4 flux (A = 7155.6, B = 11.0168) of approximately 10 to 100 times the Ga flux. These mathematical expressions have proven useful in deriving target temperatures in setting up oven operating levels. Experimental deposition conditions for a growth rate just under one $\mu m\ hr^{-1}$ in the system at Georgia Tech (Figure 2, page 17) are s = 0.377 cm, h = 5.5 cm, T_{Ga} = 1000 °C, T_{As} = 300 °C, T_{sub} = 600 °C, and a system pressure (As_4) = 4×10^{-7} Torr.

A number of dopants for GaAs grown by MBE have been investigated. Sticking coefficients for p-type dopants are generally much smaller than for n-type dopants. Using high beam fluxes, Mg has been incorporated as a p-type dopant[21], while tin and silicon have been employed for n-type doping[18]. Either type of doping can be realized using Ge, depending upon the surface configuration during epitaxial growth[15]. If the surface is As-stabilized, n-type layers result. Germanium incorporated under Ga-stabilized surface conditions gives p-type layers. When GaAs films are grown in MBE without intentional doping, they generally show p-type behavior.

It should be emphasized that MBE provides considerable flexibility in achieving prescribed doping profiles. Since doping is primarily a function of the deposition rate during epitaxial growth, this rate may be adjusted

gradually by changing the temperature of the dopant cell or the rate may be abruptly altered via the shutter control.

2.2 MBE SYSTEM DESCRIPTION

2.2.1 Basic System

Figure 2 presents a schematic of the basic MBE system for growing multilayer devices as it was originally designed and implemented. A number of significant modifications have been incorporated in this design. The original system will be described here and the modifications in the following sections.

The major components of an MBE system are the source flange, substrate heater flange, the monitoring and control equipment, and the vacuum system. The vacuum system used for the MBE work is a Varian 360 with cryogenic roughing and has not been modified during the first year. The source flange is shown in Figure 2. Composite alumina and graphite source furnaces are mounted horizontally on a standard 8.0 inch flange. Power input to the gallium source is derived from a programmable power supply that is regulated by a controller which in turn is driven by a thermocouple imbedded in the oven. Shutters located between the ovens and the substrates allow rapid selection of the required combination of effusing flux species. Three heated substrate positions were available on the original substrate heater flange. Individual substrates were moved vertically in sequence to the growth position while the other inactive positions were appropriately shielded. A thermocouple attached to the thin film Ta on BeO substrate heater was used to monitor temperature and provide a signal for temperature control. A liquid Ga interface was used for good thermal contact between the substrate and the substrate heater. The control package used for the source furnaces and substrate heaters is a Leeds

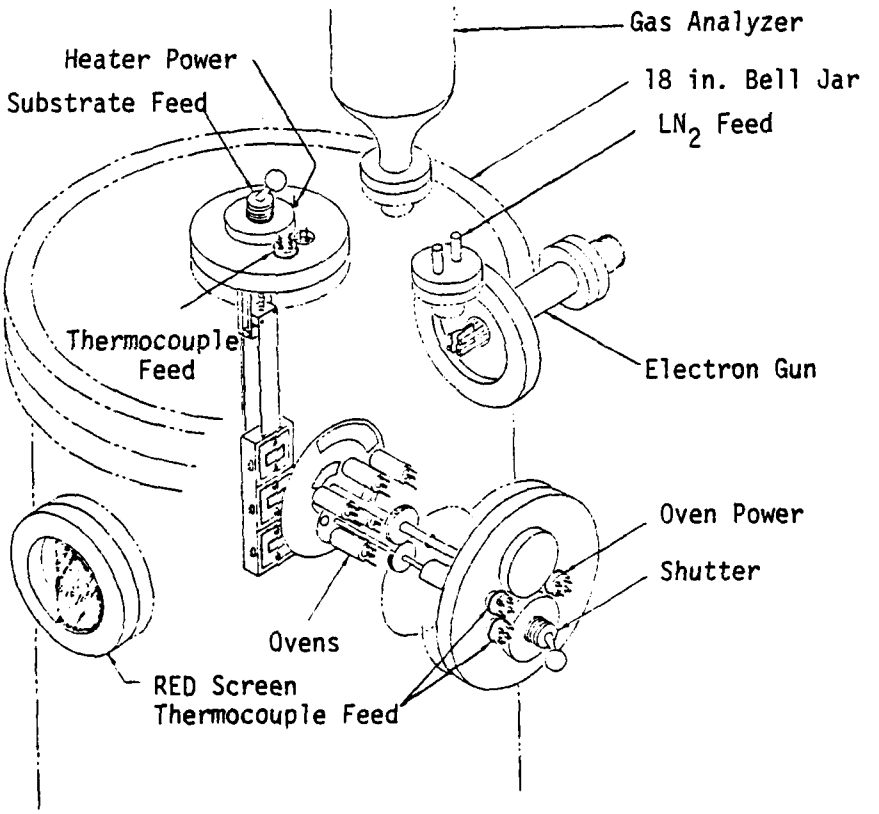


Figure 2. MBE System for Growing Multilayer Devices

and Northrup Electromax III with a Hewlett Packard model 6286A programmable power supply. Other monitoring and control equipment includes a monopole residual gas analyzer for the identification of gaseous components in the system before, during, and after growth and an electron gun for surface studies. The beam from the electron gun (0 to 20,000 eV) is adjusted for grazing incidence upon the substrate surface. Reflection electron diffraction patterns formed on the fluorescent screen directly opposite the gun permit the surface structure of the deposited layer to be determined in situ.

When the As source is heated, its temperature determines the system pressure. The As flux is also dependent on time and it is often necessary to increase the source temperature 20 °C during a given run in order to maintain a constant As pressure or flux. Therefore, an automatic pressure control was installed to maintain a constant As flux. The ion gauge drives a servo with a potentiometer that feeds a signal to the As oven power supply. The control is very good and the system can be left unattended after the run is started.

2.2.2 Source Flange Modifications

Many epitaxial layers were grown with the MBE system as described above and this work revealed several design changes in the source flange assembly that would improve operation and reliability. A complete new source flange assembly was designed and built to minimize system down time during change over. The desirable features incorporated in the new flange were: individual source shutter control, a cold trap which encloses the volume between sources and substrate, and fixed pointing of the source cells.

Figure 3 is a picture of the new source flange and Figure 4 is a picture of the major component parts, i.e., the 8 inch vacuum flange with necessary feedthroughs, the source furnace orienting tubes, and the liquid nitrogen trap.

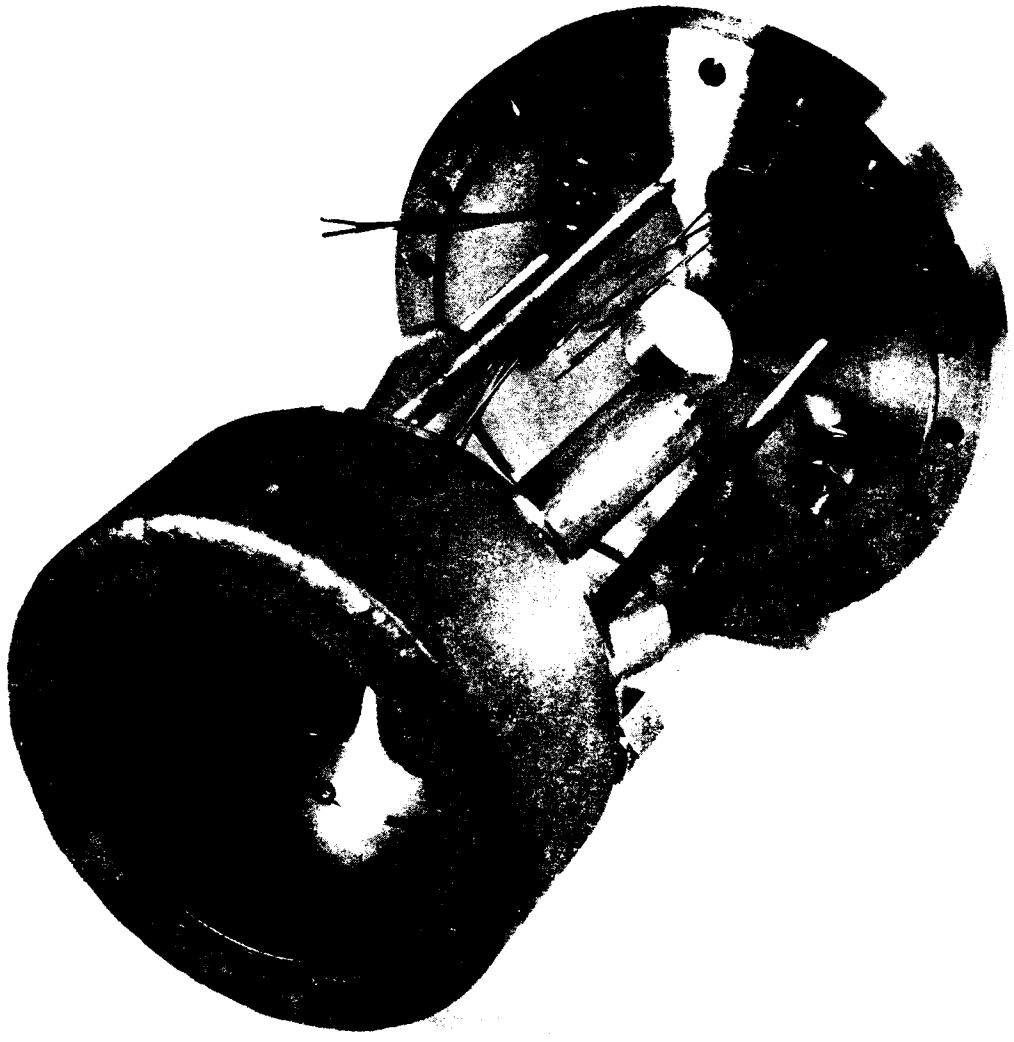
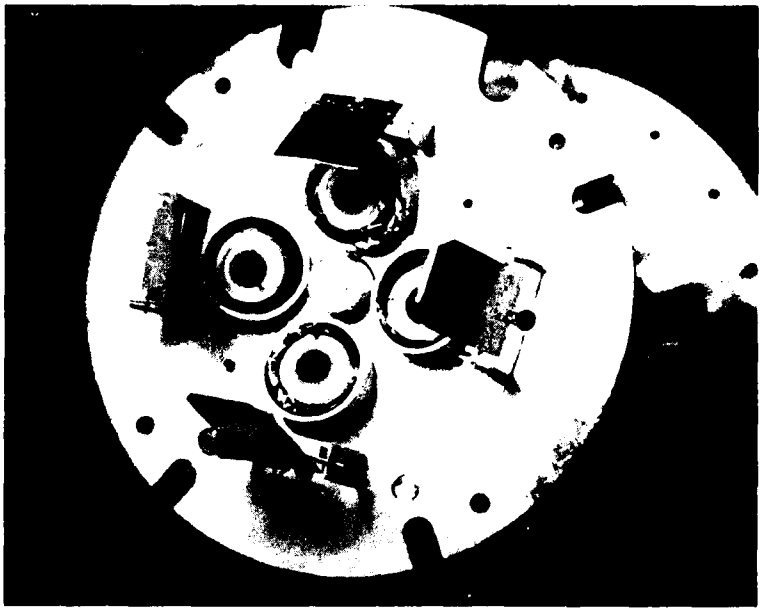


Figure 3. Source Flange Assembly for MBE System

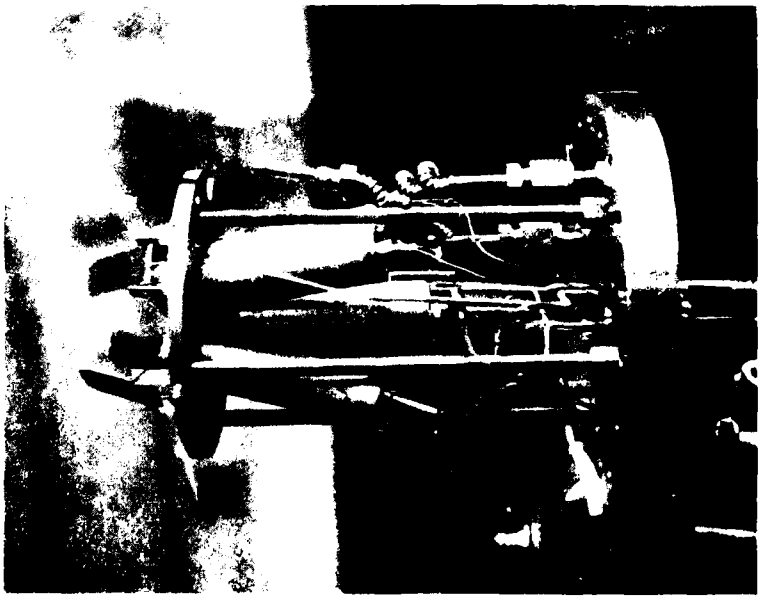
Figure 4. LN_2 Trap, Oven Pod Assembly, and Flange for MBE Sources.

The shutters are not shown in these pictures, but cover the ends of the source tubes and work like a foot-actuated trash can lid. The central hole in the 8 inch flange allows passage of the shutter control rods which are housed in individual tubes and driven by a steel slug with an external magnet. Each source is held in proper orientation by a 1.0 inch diameter stainless steel tube. Some thermal isolation is provided by these tubes, since they have a conduction path to the cold trap, but most of the isolation is accomplished by wrapping the sources in several layers of dimpled Ta foil before they are slipped into the orienting tubes. The cold trap encloses the volume between the source cells and the substrate and thereby isolates this volume to minimize effects from the rest of the vacuum system. An automatic LN_2 fill is used to keep the trap filled at all times during growth. Some fluctuation in the water vapor peak can be seen on the RGA when the LN_2 in the trap is allowed to get low. The automatic fill also allows the operator to leave the system after conditions are correctly set and growth is started. Even overnight runs would be possible, if necessary, for a thick or slow growth layer.

Another major change was the addition of a much larger As oven. The new As source was positioned in the center of other sources as shown in Figure 5. The construction features that distinguish this oven from the remaining ovens used for the higher temperature evaporants are the large capacity, the elimination of the graphite liner, and the use of a heated snout aimed at the substrate. Only the heated "snout" can be seen at the center of the support fixture in Figure 5. The reason for the large As source is explained in Section 2.3.4. The shutters originally used in the MBE work were made of stainless steel, but it was found necessary to eliminate all



(a)



(b)

Figure 5. Modified Source Flange with Large As Oven and Ta Shutters.

stainless steel components in the system that got hot during epitaxial growth. Therefore, Ta shutters were constructed and installed to replace the stainless steel. The Ta shutters can be seen in Figure 5 which shows the source flange before installation of the LN_2 trap. The oven shutters on the source flange connect to iron armatures that are actuated by eight electromagnetic drive coils shown in Figure 6. The coils operate in pairs - one coil opens the shutter, the other coil closes it. The electromagnets

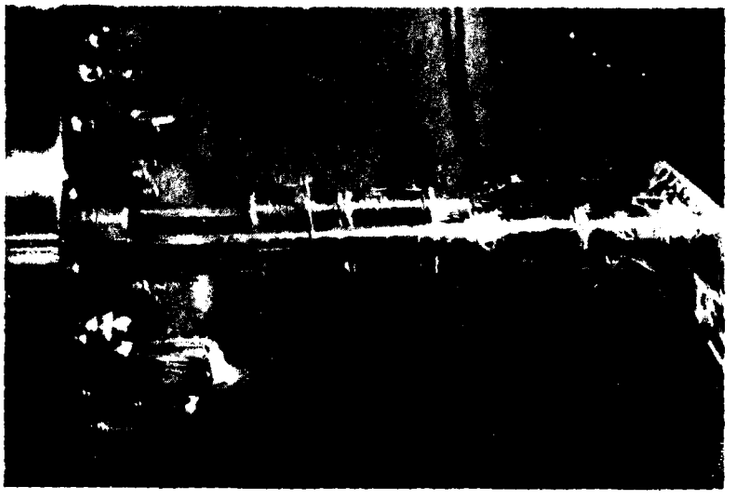


Figure 6. Detail of Electromagnets Driving Oven Shutters

are fed from a central distribution panel. Protective circuitry has been introduced which prevents unintentional shutter operation. A given coil cannot be energized until a second switch has been armed.

2.2.3 Substrate Heater Modifications

There are several very basic but difficult problems associated with the substrate heater. It is difficult to determine the substrate temperature accurately, because growth temperatures are too low for optical methods and thermocouple contacts are very unreproducible in vacuum. The substrates are mounted on a carrier plate or directly on thin film heaters using a liquid-metal interface such as Ga or In for good thermal contact. Either the substrate heater or the carrier plate must be easily demountable to make changing samples as quick and simple as possible. Thus, either the thermocouple contact or the heater power contact or both must be broken for each substrate change. If the thermocouple is mounted on the carrier plate it is exposed to the molecular beams and is subject to alloying changes. If it is mounted remotely there is little correlation between control temperature and sample temperature. Sample positioning must be reproducible (particularly for electron diffraction studies), but cannot be rigid because of thermal expansion. Also, the substrate heater must be easily cleaned and provide no undesirable doping source for the epitaxial layers being grown.

It is desirable to grow the epitaxial layers under the best UHV conditions that are practicable. Thus, after the system is opened to add substrates or source materials, an overnight pumpdown is generally necessary to achieve a pressure of 5×10^{-9} Torr or less where most of the runs were started. A three position heater was used initially to maximize the benefit of each pumpdown. Several models of the three position heater were tried in attempting to solve the basic substrate heater problems mentioned above. The first design was sputtered Ta thin film with sputtered Au contact strips

on a BeO substrate. The temperature uniformity and thermal response time were excellent, but this heater was demounted for each substrate change. Thermocouple contacts were not reproduceable and the power contacts were not reliable for this model. The same heater was used for the second model, but the substrates were mounted on the BeO carrier plate which was held against the heater by spring tensioned Ta wire loops at opposing corners. The heater contacts were more reliable, but thermal response time and temperature uniformity were worse for the multiple plate assembly. This multiple plate heater had the control thermocouple mounted between the heater and carrier plates. Poor agreement was obtained between this thermocouple and one mounted on the top surface of the carrier plate. Here, temperature variations between runs of up to eight percent were observed and thermal drops of 140 °C were typically encountered between the inner and outer thermocouples. The growth results indicated that temperature gradients across the specimen were also larger than those observed for single plate heaters. Figure 7 is a picture of the third three position assembly. One station is complete with the BeO thin film heater in place; another shows the molybdenum support plate, electrical contacts and thermocouple position; and the third shows the leaf springs that hold the heater and thermocouple in position. The thermocouple fits into a hole drilled into the bottom center of the 0.125 inch thick BeO heater. The heater was checked by heating above 600 °C so the thermocouple temperature reading could be compared with the optical glow of the heater. The heater contacts performed well, but the thermocouple temperature reading was 200 °C lower than the optically observed temperature

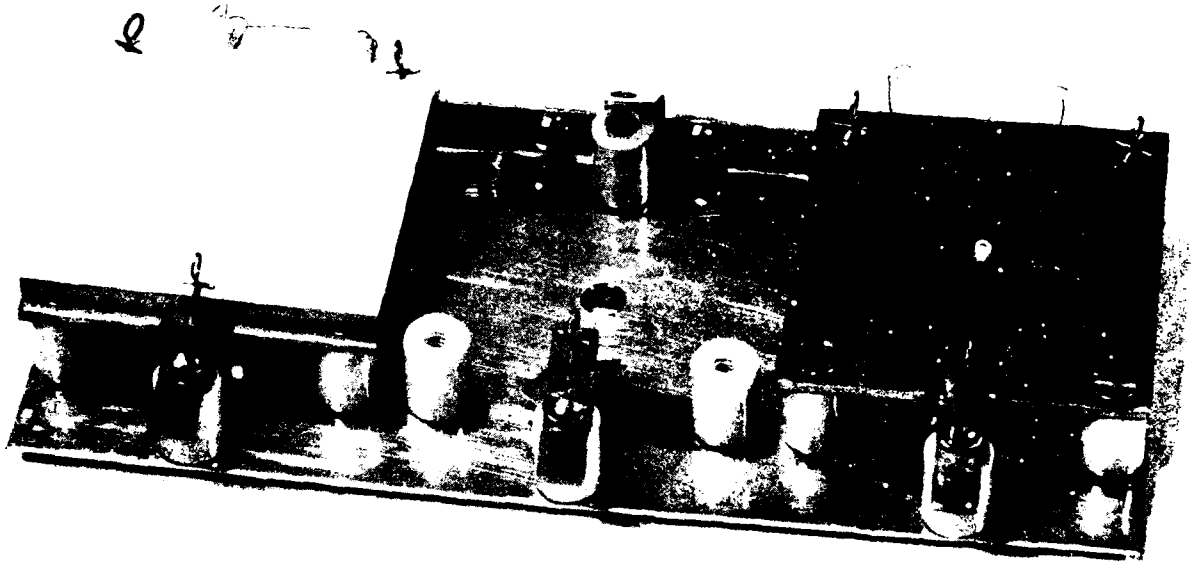


Figure 7. Closeup of Partially Assembled Substrate Heater Assembly

of the heater surface. The thermocouple position and connection was therefore changed to a C-clamp type fixture that holds the thermocouple firmly against the top surface of the BeO. This clamped contact worked well and was used for numerous MBE runs.

The runs made using the BeO substrate heaters all had a high n-type impurity level, thus other materials were tried for the thin film heater substrate including vistal (Al_2O_3), pyrolytic boron nitride, and fused quartz. Of these three materials, fused quartz was the most thoroughly evaluated.

The introduction of a cold trap that surrounds the volume between the source ovens and substrates had no noticeable affect on the doping level for background concentrations above 10^{16} cm^{-3}. The system components within this volume, therefore, were believed to be the most probable source of the background impurities that were being incorporated in the epitaxial layers. Therefore, a single position substrate heater was constructed that could be baked out at high temperature before installation in the MBE system. Tantalum, alumina, and fused quartz were the only materials used in construction, except for springs that apply pressure for the electrical contacts. These springs cannot be baked out at high temperature, but are isolated and shielded from heat during operation. A picture of the assembly is shown in Figure 8. The fused quartz/Ta film heater assembly irradiates the back side of a Mo carrier plate. A liquid metal interface of In or Ga holds the GaAs substrate on the front surface of the Mo plate. The thickness of the Ta film is uniform under the Mo plate, but increases toward the ends where the spring clamps make electrical contact for power.

In this way the contacts are kept cool and heat is concentrated under the substrate carrier plate. The thermocouple is spot welded to a Ta washer which is clamped to the Mo carrier plate with a Ta screw. The Mo carrier plate is mounted directly on the fused quartz with an indium interface. While this substrate heater design contained a number of desirable operating characteristics, there was evidence that chemical reduction of the hot fused quartz contributed a residual background donor concentration of $10^{15} - 10^{16}$ cm^{-3}.

The substrate heater which has consistently yielded the greatest freedom from unintentionally induced heater contamination is illustrated in Figure 9. Thermal radiation from a resistive Ta filament is used to heat a Mo plate carrying the GaAs substrate. Additional construction features of this heater shown in Figure 9 include the extensive use of Ta support stock and two 0.030 in diameter alumina rods holding the Ta filament winding in position. A chromel alumel thermocouple is attached to the 1.0 x 1.0 inch Mo carrier plate by a Ta screw. A substrate temperature of 600 °C is obtained with an input power of approximately 40 watts. Swinging catches at the corner simplify the installation and retrieval of the carrier plates.

2.2.4 Interlock System

The primary reason for the interlock system is for Schottky barrier studies. The freshly grown epitaxial layer can be metallized before it is removed from the vacuum system, producing a clean interface to study. In addition, however, the interlock decreases pumpdown time and keeps the sources under vacuum while the new substrate is placed in the system.

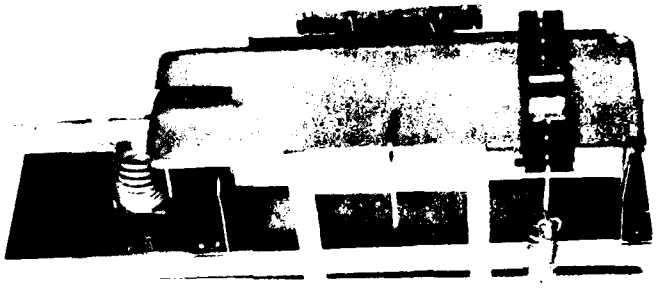


Figure 8. Bakeable Substrate Heater Assembly

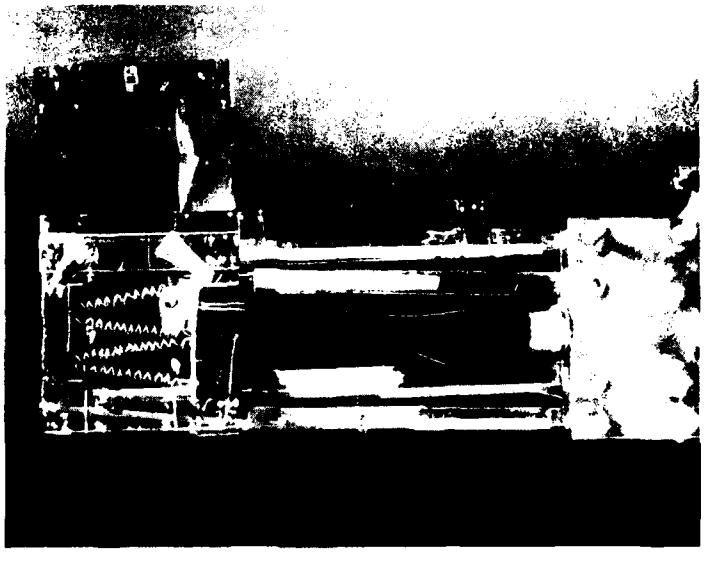
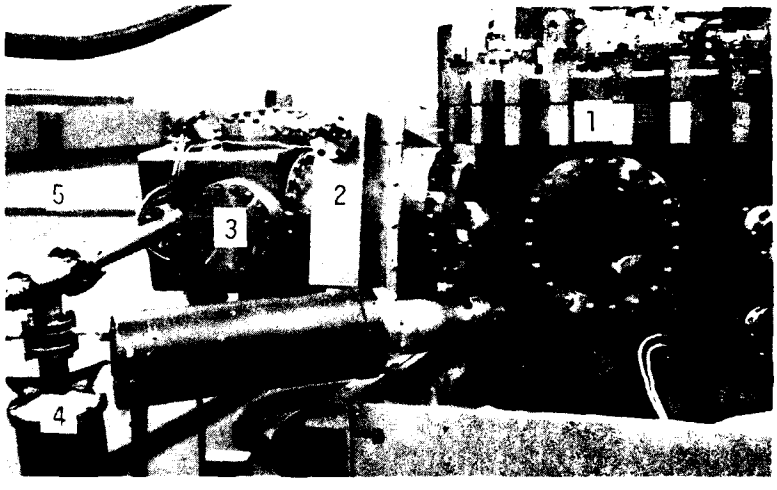


Figure 9. Modified Substrate Heater Assembly

Figure 10 is a picture of the interlock assembly mounted on the MBE vacuum chamber. The components are numbered: 1) the main MBE growth chamber, 2) interlock valve, 3) interlock chamber with evaporator unit for metallization of samples, 4) cryogenic roughing pump, and 5) metal tube housing for the magnetic armature and rod that provides the motion necessary for sample insertion. The substrate heater and insertion rod are shown partially extended in Figure 11. The coil contains a bundle of five wires (a spring steel support wire, two copper power leads, and a thermocouple) necessary for substrate heater operation and can be extended the 18 inches necessary to move from the interlock chamber metallization position to the growth position in the main chamber. With the interlock valve closed, the main chamber can be maintained at a vacuum of 3×10^{-9} Torr while a new substrate is placed in the interlock chamber. After the interlock chamber is cryogenically pumped to a pressure of a few microns and the valve opened the main system pressure increases immediately to 10^{-5} Torr. In a matter of minutes, however, the pressure is below 10^{-7} Torr and in four hours it is below 4×10^{-9} Torr. The interlock system has therefore eliminated the overnight pumpdown that has been necessary to achieve the starting pressures that have been customarily used for the MBE growth runs.

In order to take full advantage of the interlock system, it is necessary to have sufficient source material in the system for several weeks of operation. The original As source based on the Ga and doping oven design would only last about 10 hours at growth conditions. Therefore, a large As source was designed that holds 30 times more As. The proportionate increase in the As source lifetime is even greater since the larger source is



1. MBE Growth Chamber
2. Interlock Valve
3. Interlock Chamber
4. Roughing Pump
5. Insertion Rod Housing

Figure 10. Interlock Assembly Mounted on MBE System

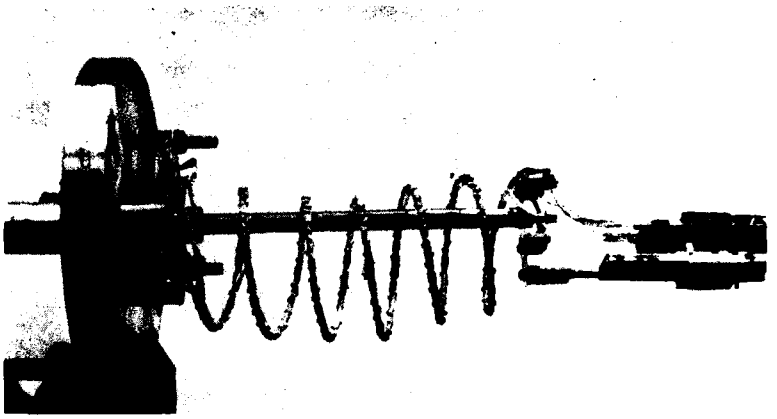


Figure 11. Substrate Heater and Insertion Mechanism

prebaked to remove the arsenic oxides only when the oven is reloaded with fresh As.

It is particularly significant that the combination of the interlock and the larger As oven has, after several hours of oven operation, greatly reduced the strengths of the various oxides of arsenic that were normally observed in the 0 to 300 amu range monitored by the residual gas analyzer. Only a trace of AsO (91 amu) exists now where previously this component was comparable to the sometimes larger than the residual species H_2O at mass 18, CO at 28 and CO_2 at 44. This is a direct result of better vacuum management since the highest pressure of atmospheric constituents reached in the main

chamber is 10^{-5} Torr and this lasts only a few seconds following the opening of the interlock gate valve. Sample throughput has also been enhanced.

2.3 OPERATION PROCEDURES

2.3.1 Substrate Preparation

The condition of the substrate surface prior to epitaxial growth is very important in determining the quality of the grown layers for all methods and types of epitaxial growth. Careful surface treatment is particularly important for MBE, because there is no opportunity for an in situ etch such as is normally done with CVD to remove several microns of GaAs.

The substrates used for this work were all purchased from Laser Diode Laboratories. Most of them were purchased already polished, but a few were polished here at Tech using a dilute Clorox solution and a rotating table with a nylon cloth cover. All substrates were subjected to a very careful cleaning procedure immediately prior to loading in the system. The cleaning procedure that has been used thus far for the preparation of substrates has been used successfully for many years in this laboratory for the growth of CVD GaAs epitaxial layers. This cleaning procedure (Table 1) is essentially the same as that reported by Cho and Hayashi[58] and leaves the surface preferentially covered with oxygen rather than carbon. The oxygen is reportedly[57] easily desorbed by heating to approximately 530 °C, but carbon contamination must be removed by other techniques such as argon ion sputtering.

2.3.2 Processing Sequence

The fundamental processing sequence of MBE layers can be divided into five steps; namely, substrate cleaning, predeposition operations, layer deposition, post deposition operations, and layer evaluation. Substrate

cleaning procedures for the mechanically polished substrates are given in Table 1.

Table 1. GaAs Substrate Cleaning Procedure

1. Vapor degrease in boiling trichlorethylene vapor.
2. While still in tri vapor, rinse with methanol and keep covered with methanol until blown off with dry nitrogen.
3. Etch 1 minute in H_2SO_4:H_2O_2:H_2O, 5:1:1 and rinse in hot DI water.
4. Rinse in methanol and keep wet until Br etch.
5. Etch 1 minute in Br;methanol 1:50.
6. Rinse in methanol.
7. Blow dry with N_2.
8. Rinse in hot DI water.
9. Blow dry with N_2.

Predeposition operations in a vacuum environment consist of outgassing ovens and the substrate heaters, minimizing carbon buildup within the

vacuum system during pumpdown, and operation of the As oven during extended substrate heating to temperatures $\geq$ 400 °C. The latter step minimizes thermal etching of the GaAs substrate. Temperatures of ovens and substrates are monitored during the layer deposition. In addition, an ionization gauge tracks system pressure. An analysis of the gaseous products using the monopole reveals that the primary component is As_4. There is some As_2 or doubly ionized As_4 and relatively smaller amounts of As and As_3. Traces of H_2O, CO, and CO_2 can be detected. Post deposition operations in the vacuum system involve cooling the substrate in an As atmosphere to minimize thermal etching. A final heating is conducted at 350 °C and low residual background to desorb any remaining As from the grown surface. General structural characteristics for deposited layers are evaluated in situ using RHEED. Other structural diagnostics applied to the layers include SEM, RHEED (100 keV), Auger and X-ray analyses. Fundamental electrical properties are determined by Hall measurements and capacitance-voltage data from Schottky diodes formed on epitaxial layers. The latter are used to characterize the underlying doping profile.

2.3.3 Auger Electron Analysis

Auger electron analysis was used during the early part of the program to study the condition of the substrate surface before layer growth. The chemical cleaning procedure given in Table 1 was studied along with a modified version that omitted steps 8 and 9. In each case the Auger spectrum was taken as soon as possible (background pressure of 8×10^{-7} Torr in 2 hrs.) after loading the samples in the vacuum system.

The initial scans are shown in Figure 12 and 13 and no difference is seen between the two cleaning procedures. No carbon is detected, but a very large

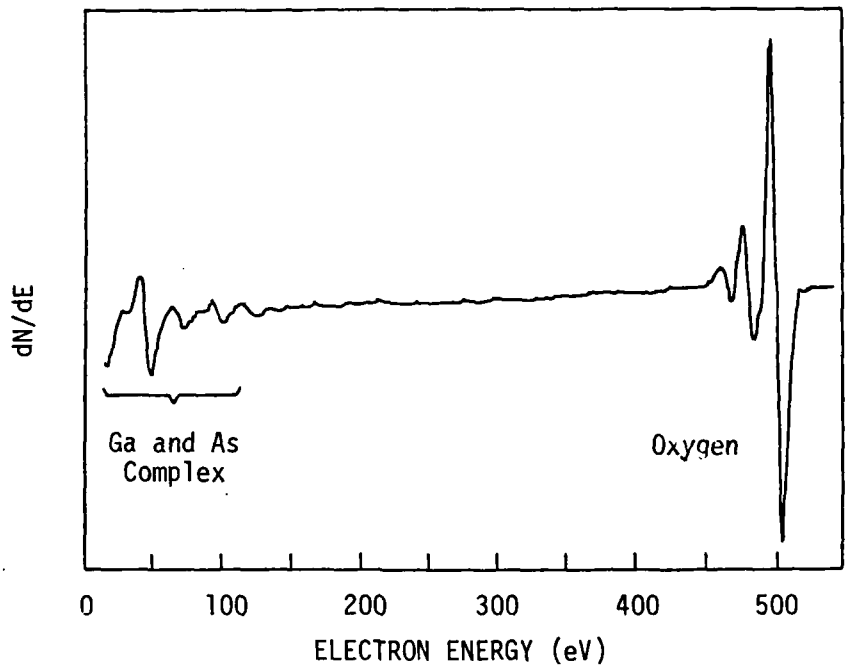


Figure 12. Auger Spectrum of GaAs Surface with Hot DI Water Final Rinse

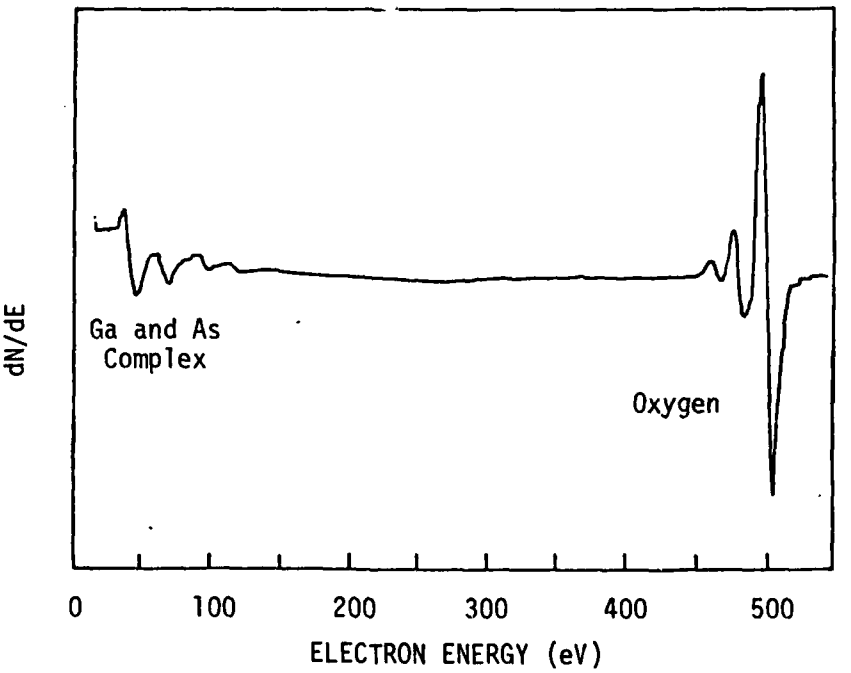


Figure 13. Auger Spectrum of GaAs Surface with Methanol Final Rinse

oxygen peak is observed. This is the type of surface the cleaning procedure is supposed to produce. Figure 14 is a spectrum taken after overnight exposure to the vacuum environment. The carbon peak-to-peak height increased to 2.4 cm and the oxygen peak decreased to 4.9 cm as would be expected for an overlayer of carbon on the oxide. Heating to 600 °C in the system reduced the oxygen peak to 2.1 cm, but the carbon peak was essentially unchanged. Sulfur and nitrogen peaks also appeared after heating. This data confirms that the surface oxides left on the GaAs after the cleaning procedure are volatile and greatly reduced by heating in vacuum. It also indicates that the amount of surface carbon on the GaAs substrate is determined more by the time of exposure to the vacuum than by the cleaning procedure and once formed the carbon is not affected by heating. Sputtering would be required to remove the carbon and then annealing to remove lattice damage introduced by the argon ion sputtering.

An experiment was also made to determine whether substrate material exposed to the vacuum environment for three days before growth had more carbon at the substrate interface than a substrate exposed for only a few hours. Approximately 500 Å of GaAs was grown on both substrates. The available Auger system is presently unable to ion mill and make Auger analysis simultaneously. Thus, to expose the interface the overgrowth of GaAs was sputter etched and analyzed in successive increments. The low energy of the Auger response of carbon complicates the task because of the small escape depth of the electrons. Several attempts at this stepwise process failed to produce a carbon response and further work was abandoned.

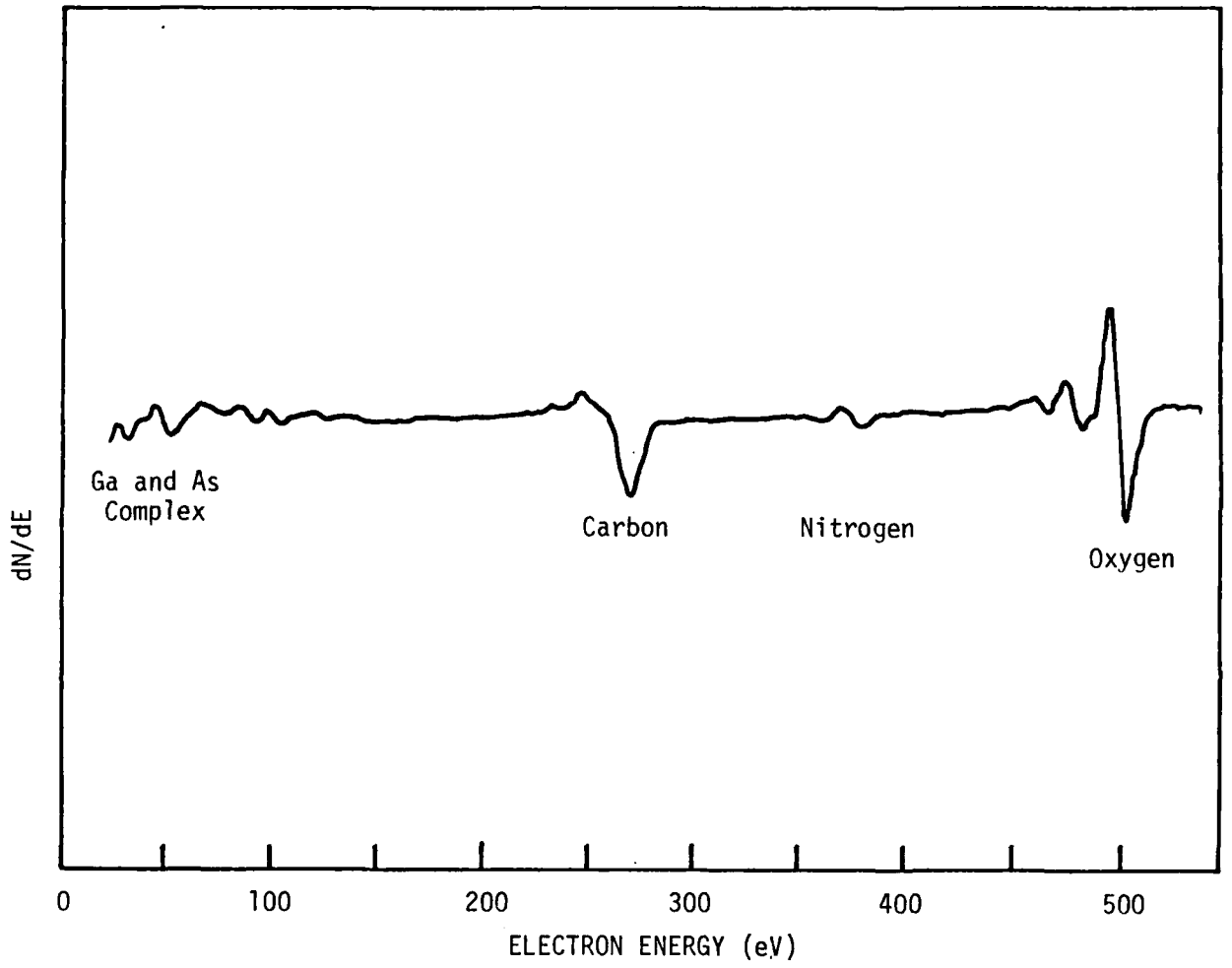


Figure 14. Auger Spectrum of GaAs Surface After Exposure to Vacuum Environment Overnight

2.3.4 X-ray Analysis

A number of X-ray topographic techniques have been investigated with the twin objectives of identifying superior GaAs substrates and of studying the characteristics of defects induced in the epilayer overgrowth as the deposition parameters are varied. The results of back-reflection Laue analyses, Berg-Barrett analyses, Laue Reflection Topography and Scanning Reflection Topography are described below.

Back-reflection Laue photographs are taken to determine the crystallographic orientation of the substrates with respect to the wafer geometry of the samples. One of the Laue photographs can be seen in Figure 15. The 4-fold axis (100) is approximately normal to the plane of the sample. Also note the large degree of non-Bragg scattering about the incident beams. To avoid completely fogging the film and losing the diffraction pattern, these back-reflection Laue photos had to be taken with the high-voltage setting of the X-ray generator reduced to 15 or 20 kV. As it turns out, this parasitic scattering also showed up and proved to be a problem in Berg-Barrett studies.

The Berg-Barrett (BB) technique illustrated in Figure 16 was appealing because the simplicity of the technique and equipment should theoretically enhance the rapid examination of many samples and the reflection geometry would be more useful in view of the high absorption characteristics of GaAs. More than 30 BB photos were taken of two GaAs samples. These photographs were taken with different radiations (Mokα and CuKα), different high-voltage and beam current settings, and different Bragg reflections. Initial attempts at BB photography with Cu radiation failed, because the high parasitic scattering did not permit accurate alignment of the Bragg

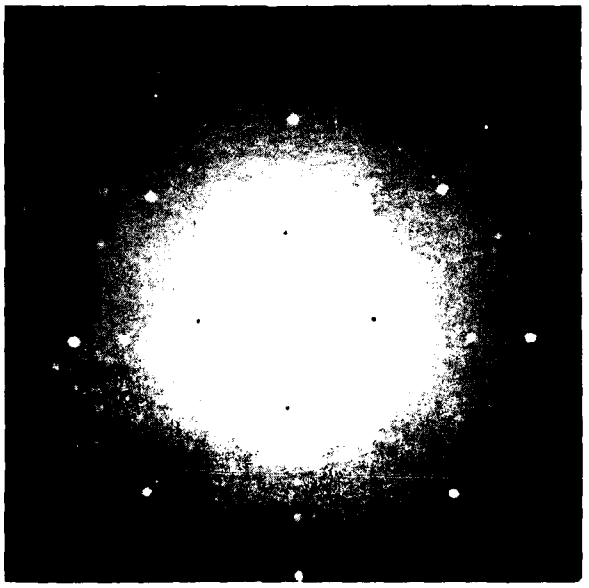


Figure 15. Back-Reflection Laue of GaAs Substrate

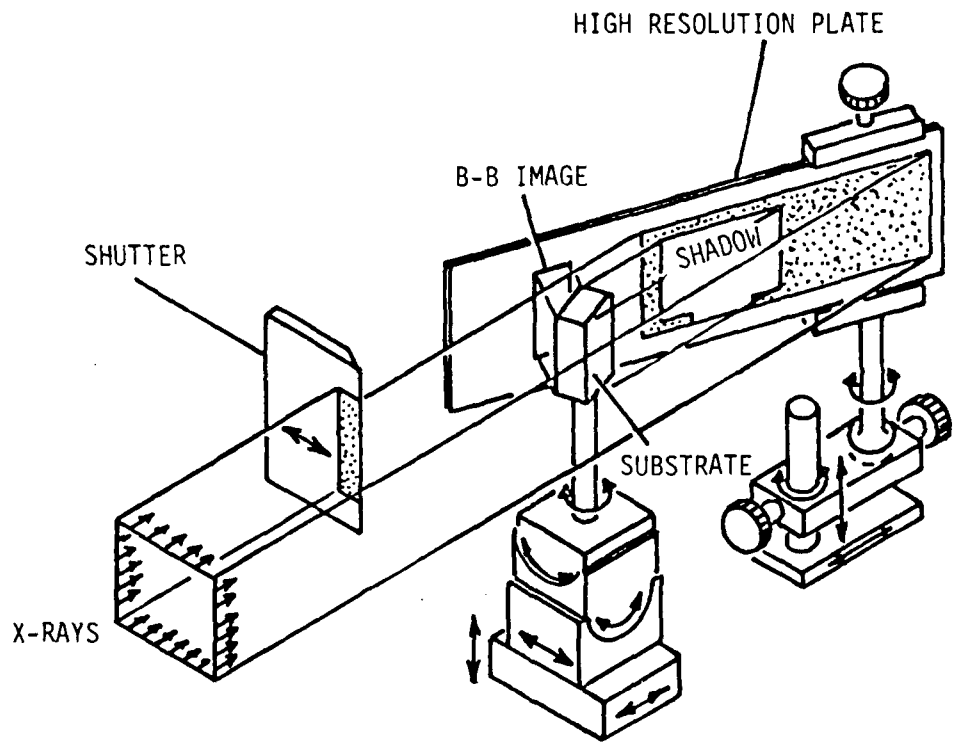


Figure 16. Diagram of Component and Diffraction Geometry for Reflection Berg-Barrett X-ray Diffraction Topography

reflections. The various Bragg reflections could be found with MoKα radiation, but due to the shorter wavelength (0.71 Å *vs* 1.54 Å), the "ideal" BB geometry could not be achieved. The results of these experiments led to the following observations on ways to deal with the parasitic scattering problem:

1) the use of lead slits to allow only the diffracted beam of interest to strike the photographic plate,
2) the use of slits implies that a scanning technique must be used in order to examine reasonable sized areas of the samples, and
3) a reflection rather than transmission technique must still be employed because of the absorption of the samples.

The use of a reflection scanning technique adversely effects the sample throughput because set-up times and exposure times are increased.

Laue Reflection Topography (LRT) was tried without filters for several exposure times with both X-ray and Polaroid film. In concept, this approach is very simple. The entire sample surface is flooded with X-rays and a back-reflection Laue photograph is taken. When examined in detail, each Bragg spot is a topographic image of the sample surface. Application of this technique, however, to the GaAs substrates yielded only fogged films with no diffraction information.

Implementation of the scanning technique in conjunction with Ni filters did lead to successful topographs. In Scanning Reflection Topography (SRT) special equipment is employed to translate the sample and film (in synchronism) through the diffracted X-ray beam. Initial experimental studies which varied the radiation type (Cu and Mo), the exposure time (up

to 12 hours), and the emulsion types (Kodak and Ilford L4, G5 and K5) didn't resolve the fundamental difficulty with the high background scatter. Switching to a Ni filter[59] proved to be the key element in reducing the scattering problem to manageable proportions. While it was found that the Ni filter was needed during the alignment of the crystal, subsequent work showed that adequate topographs could be obtained in about an hour without the filter (see Figure 17). Figure 17 is a print of an X-ray topograph taken of a piece of Cr-doped GaAs substrate material that was cleaned in the same manner used for epitaxial deposition. The dark area at the bottom is due to tissue paper used in the sample holder, but several other interesting features can be seen, some of which have been correlated with features seen in polarized optical micrographs. The semicircular contrast features seen at A and B are due to strain fields created by nonuniform etching where the sample holder gripped the substrates during the chemical cleaning operation. Features at C and D which were also seen with polarized optical microscopy are massive defect structures which can still be observed after the substrate is etched and a partial epilayer deposited on it. Figure 18 is a print of the X-ray topograph taken of the same piece of GaAs as that used for Figure 17. after the etch and epilayer deposition. The epilayer was GaAs uniformly doped with Ge ($\sim 5 \times 10^{16}$ cm^{-3}). The epilayer thickness (measured optically) was 1.09 micron. The dark vertical band labeled F is the epilayer boundary with the epilayer covered substrate to the right of this boundary.

Three points are immediately obvious:

1. The etching process before MBE did not relieve all of the strain due to the defects which occur at point C.

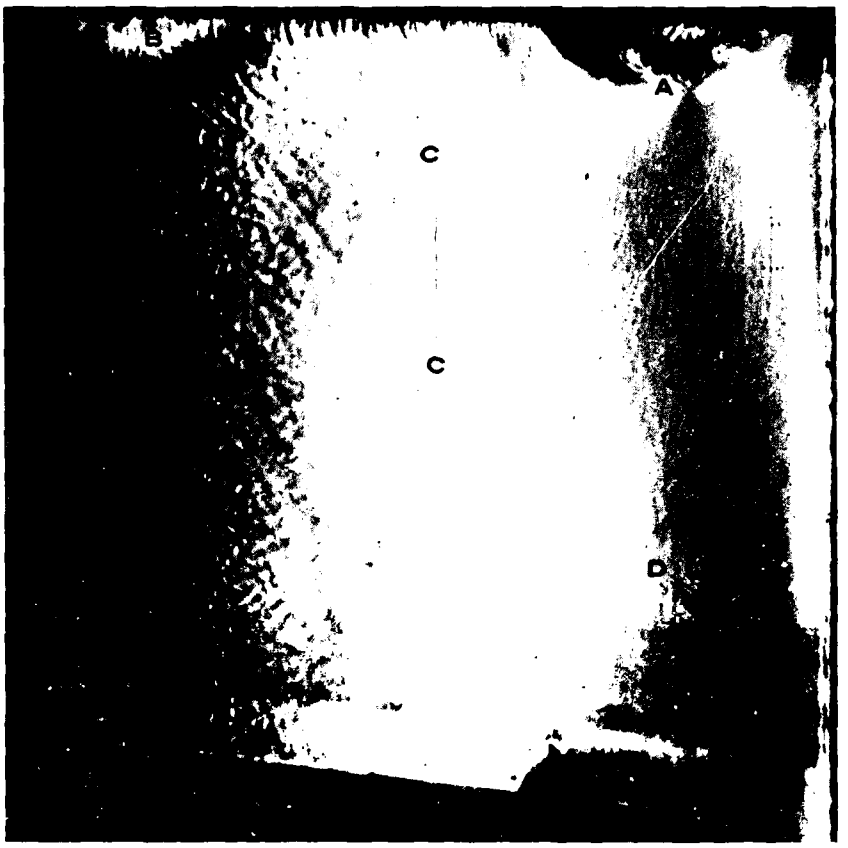


Figure 17. Scanning Reflection X-Ray Topograph of Cr-Doped GaAs Substrate Prior to Growth of the GaAs Epilayer.

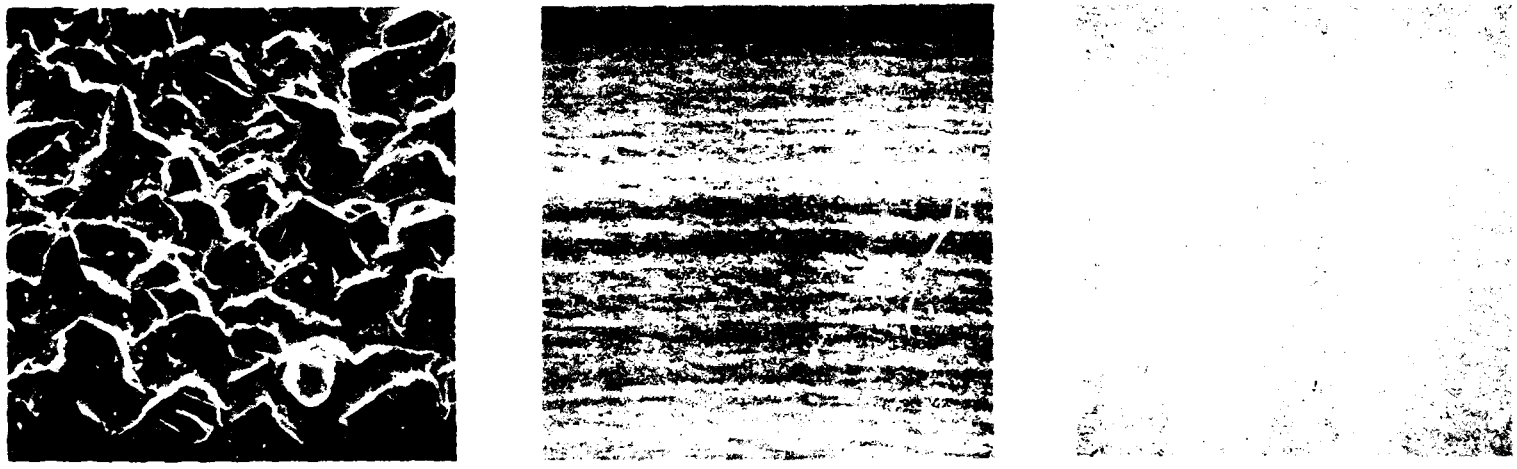
Figure 18. Scanning Reflection X-Ray Topograph of Cr-Doped GaAs Substrate with a Partial GaAs (Ge-doped) Epilayer (MBE A0315).

2. The strain fields due to defects at D can still be observed after the epilayer deposit.
3. A new defect appears after (or during) etching and epi-deposition at location E. It is not known at this time if the defect stops at the epilayer boundary or continues under the epilayer and its strain field is insufficient to propogate through the epilayer.

2.4 DEPOSITION PARAMETERS

Growth of GaAs layers on the (001) surfaces of GaAs substrates have been used to define general operating ranges for the various deposition parameters. No doping ovens were activated for this phase of the study. Temperatures for the gallium oven fell in the range of 895 to 1008 °C. The growth rate of GaAs is determined primarily by the flux of Ga incident upon the substrate. It is desirable to maintain a high incident flux of As on the substrate. Epitaxial growth was typically achieved with As oven temperatures of 300 to 375 °C. Free Ga was observed on GaAs substrates following runs with As oven temperatures of 235 to 270 °C.

Substrate temperatures were varied in a controlled fashion over the 370 to 597 °C range during a series of runs with Ga oven temperatures of 900 $\pm$ 5 °C and As oven temperatures of 360 $\pm$ 15 °C. As shown in the scanning electron micrograph in Figure 19a, growth at a substrate temperature of 370 °C is characterized by large crystallites. Many of these crystallites contain a fiber axis which is oriented at an angle of approximately 25° with respect to the (001) surface of the GaAs substrate. The large columnar crystallites have heights of 20 microns and diameters of 5 to 14



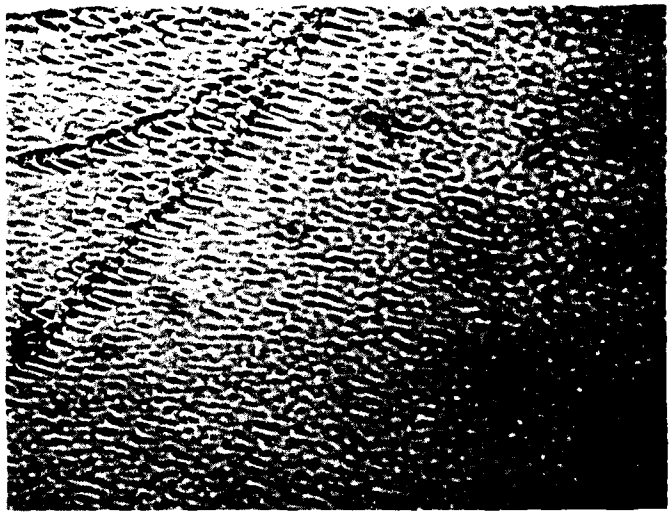
(a) (b) (c)

Figure 19. Scanning Electron Micrographs of Thick Layers (≥ 1.0 Micron) Deposited at Three Different Substrate Temperatures: (a) MBE921 I (370°C), x 520. (b) MBE923 I (540°C) x 1900, (c) MBE927 III (560°C) x 1550. The Dark Bands in (b) Arise from Microscope Instabilities.

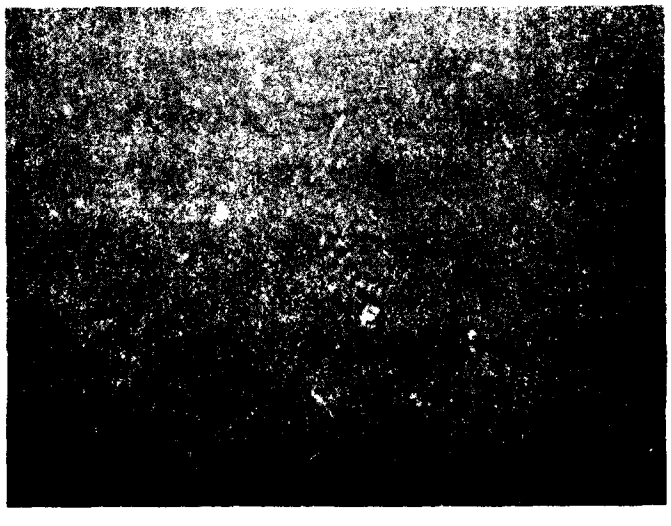
microns. Slender whiskers 20-30 microns in length and 0.5 microns diameter at the base are interspersed in the growth mosaic. As the substrate temperature is increased to 540 °C (Figure 19b), the surface features shallow undulating facets with lateral dimensions on the order of microns in extent. Finally, the surface of a layer grown at a substrate temperature of 560 °C (Figure 19c) shows a marked improvement in surface smoothness over the previous specimens.

Topographical details of smooth surfaces which show little contrast using scanning electron beams have been revealed with optical phase contrast microscopy. The substrate of specimen MBE 1020I shown in Figure 20a contained the shrinking rings of a drying stain in the left hand portion of the micrograph. It is significant that the overgrowth for both the stained and clear regions of the specimen have similar surface faceting which is generally oriented along [110] directions. This suggests that nucleated growth has occurred which is believed to be associated with surface contamination during bakeout of the vacuum system. A background pressure of 3×10^{-10} Torr was reached after a four hour bakeout. The deposition of the 0.3 micron thick layer occurred at a substrate temperature of 575 °C. Increasing the substrate temperature to 597 °C and eliminating the system bakeout (background pressure in the 10^{-8} Torr range) produced the surface shown in Figure 20b for a 1.1 micron thick layer.

The photomicrographs shown are pertinent, but are from early runs which show some surface detail. Layers are routinely grown at present with specular surfaces that are essentially featureless. Photomicrographs of these surfaces are very uninteresting and not included in this report.



(a)



(b)

Figure 20. Phase Contrast Optical Micrographs of MBE Layers. (a) MBE1020I, 500 x. Drying Streaks are Visible in the Lefthand Portion of the Micrograph. (b) MBE0130II, 500x Which was Grown Under Conditions Which Minimized Predeposition Contamination.

3.0 EVALUATION OF MBE LAYERS

3.1 ELECTRON DIFFRACTION

Electron diffraction patterns of cleaned substrates are obtained in situ with 3.0 to 18.0 keV electron beams. These patterns verify the effectiveness of the cleaning procedure and thermal desorption of the surface oxide when the substrate is heated above 500 °C. The GaAs substrates with faces 2° off (100) toward the [110] direction are normally oriented to position the electron beam along a [110] axis.

Figure 21 is typical of the diffraction patterns observed for GaAs layers grown by MBE. The streaking in the diffraction pattern along a direction normal to the shadow edge is characteristic of a surface that is atomically flat. Under this condition the Ewald sphere for the grazing electrons is in effect intersecting the reciprocal rods of a two dimensional lattice[11]. The faint "1/2-order" streaks interspersed among the primary spot diffraction streaks are evidence of a reconstructed surface structure[10,11]. Although the photograph shows a high level of incident photon light from the electron gun filament, this feature is immaterial during visual observations of diffraction patterns.

MBE specimens are also examined with 50 to 100 keV electron beams in an RCA EMU3F electron microscope fitted with a reflection electron diffraction chamber. Figure 22 shows diffraction patterns for two MBE layers for a 100 keV electron beam. Both layers are approximately one micron thick. The distinct spot patterns and the Kikuchi lines indicate a high degree of epitaxial growth with slight twinning for specimen MBE 927III. Good epitaxy is also revealed in Figure 22c for layer MBE 1030II. It is important to

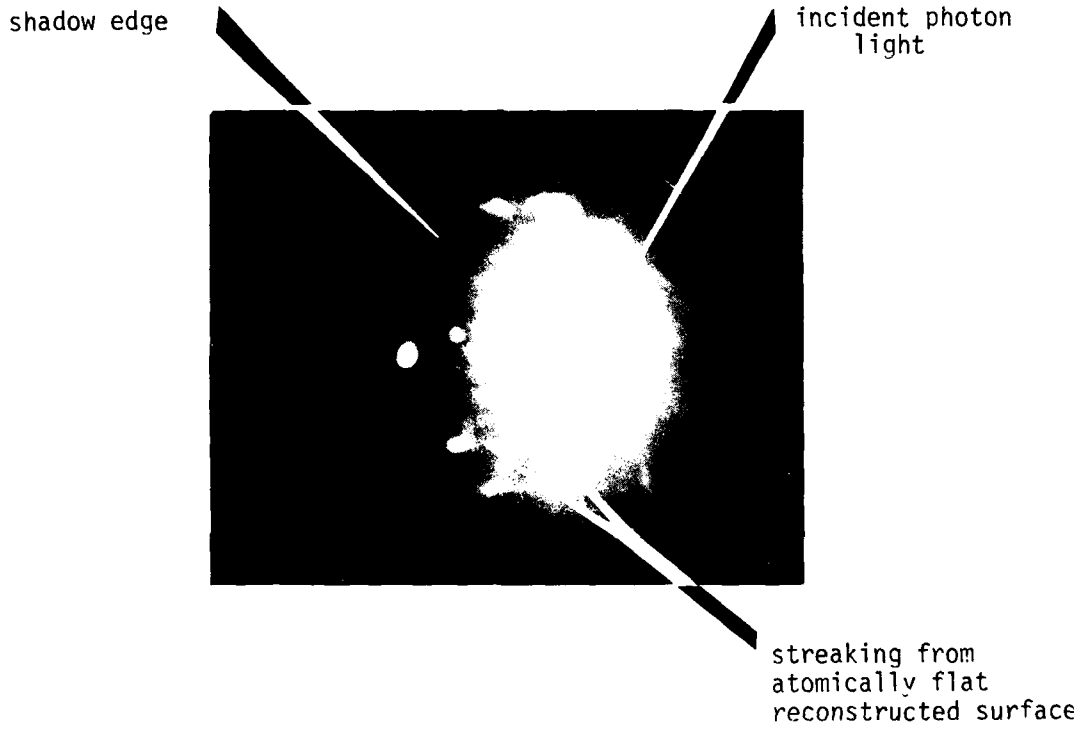
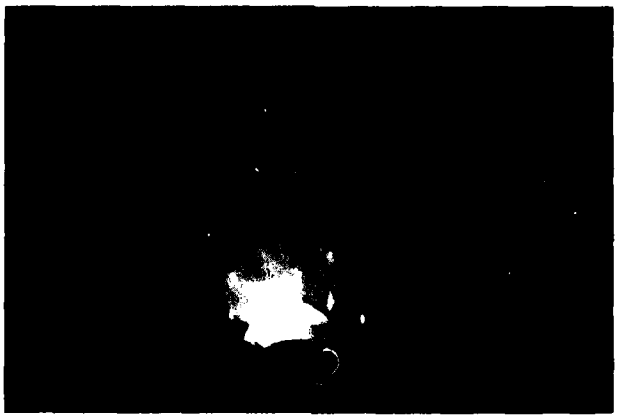
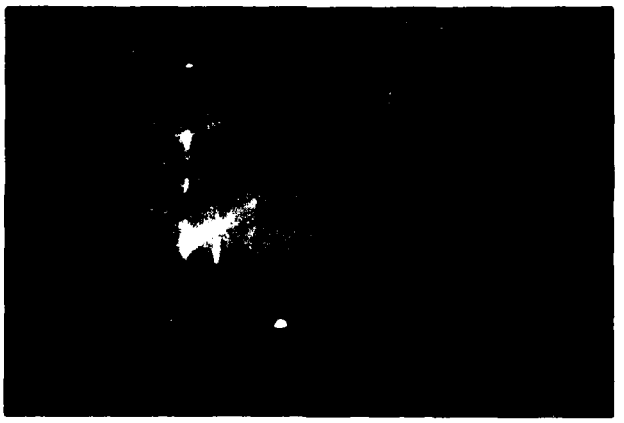


Figure 21. Reflection Electron Diffraction Pattern Obtained in situ for Thin GaAs Layer, MBE1118III (9.08 μm thick). 14.5 keV Beam, [110] azimuth. Substrate Temperature 565°C.



(a)

(b)



(c)

Figure 22. Reflection Electron Diffraction Patterns (100 keV) for MBE Layers:
(a) MBE927 III, beam along [110] axis.
(b) MBE927 III, beam along [010] axis.
(c) MBE1030 II, beam along [110] axis.

note that surface reconstruction features are not present in these samples maintained at ambient temperature. This effect has been substantiated on all samples investigated in the external microscope including layer MBE 1118III shown in Figure 21. After this layer was examined in the RCA electron microscope, it was reinserted into the MBE chamber. No pattern was observed with a 13 keV beam until the specimen temperature reached the 500 to 600 °C range. At this point a sharp, reconstructed surface pattern appeared. It is concluded that the oxide formed on the surface leads to a significant modification of the surface structure since the more energetic electron beams gave spot-type diffraction patterns for layers exposed to atmospheric pressures. A similar effect has been reported by other laboratories using auxiliary electron diffraction units to study the structural properties of GaAs grown by MBE[7,60].

3.2 HALL MEASUREMENTS

Conventional switching and d.c. potentiometric circuitry is employed to measure resistivity ρ, mobility μ, and Hall coefficient R as a function of specimen temperature. The analysis of experimental data follows the van der Pauw approach[61]. The GaAs specimens are typically scribed to a square shape (0.51 x 0.51 cm) bounded by {110} edges. A metallic evaporation defines small contact pads at the corners of the specimen. In the case of n-type GaAs epi-layers the metallization consists of thin alternate layers of Ni, Au(88%)/Ge(12%), and Ni. Briefly heating the sample to 450-480 °C alloys the contacts and provides essentially ohmic behavior. Ohmic contacts to p-type layers are realized by evaporating pads of Ag(82%)/In(12%)/Mn(6%) and alloying at 600 °C for approximately 30 seconds. Figure 23 shows typical I-V characteristics for ohmic contacts on n- and p-type GaAs.

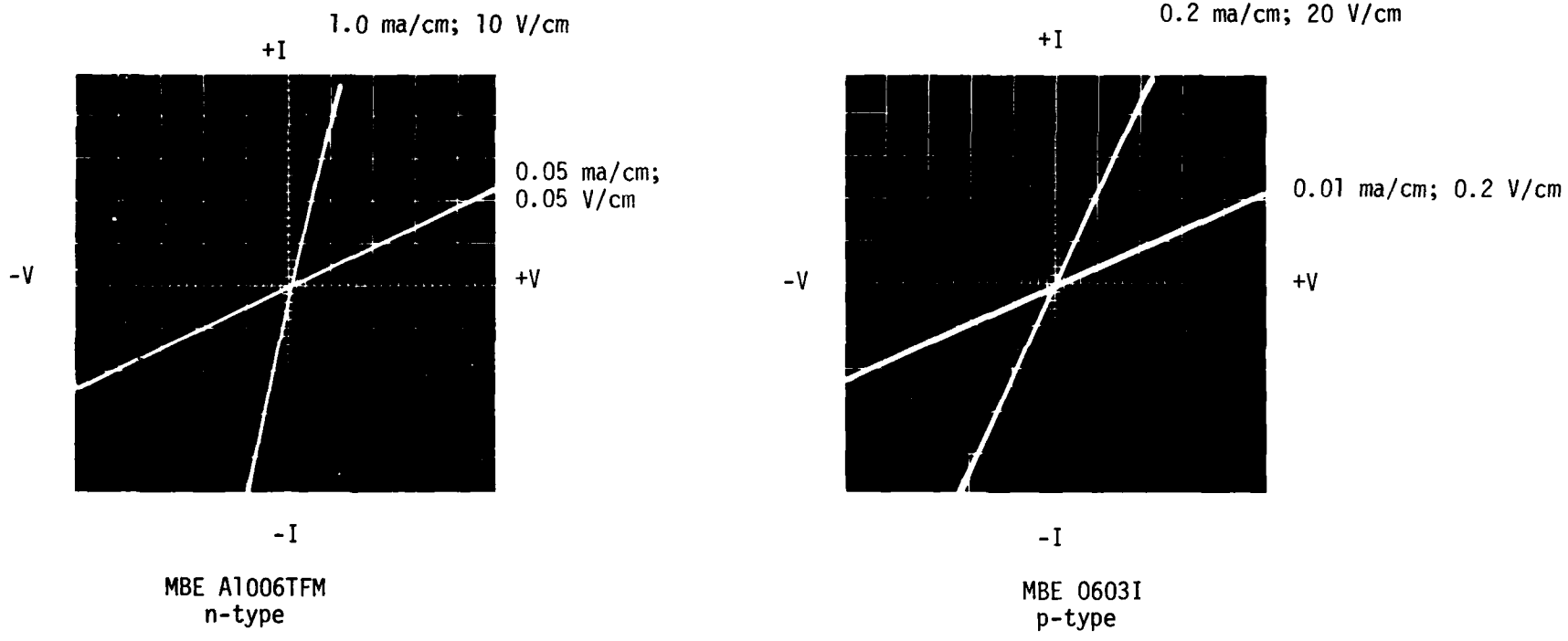


Figure 23. I-V Characteristics Illustrating the Quality of Ohmic Contacts Formed on n- and p-type GaAs. The Doping Levels in Both Layers were in the Low $10^{15}cm^{-3}$ range.

All Hall data were taken with a magnetic field of 4000 gauss. In computing the carrier concentrations for n-type samples, for example,

$$n = \frac{r}{qR} \tag{5}$$

where r = scattering factor,

q = electronic charge, and

R = Hall coefficient

the variation in r with scattering type and temperature was neglected and a constant value of unity was employed. The Hall mobility is defined as $\mu = R\rho^{-1}$. Examples of the variation in μ as a function of temperature are given in Figure 24 for two unintentionally doped MBE layers. At room temperature the p-type layer MBE 0624II has a background concentration of $6 \times 10^{15} cm^{-3}$ while the n-type layer MBE A0930 has a background concentration of $7 \times 10^{14} cm^{-3}$. The mobility variation for MBE 0624II lies close to a $T^{-2.3}$ curve determined for p-type GaAs[62] although the room temperature mobility of 322 $cm^2 V^{-1} sec^{-1}$ is lower than the 400 $cm^2 V^{-1} sec^{-1}$ reported for the highest quality p-type GaAs. Mobility versus temperature for the n-type layer follows a $T^{-1.5}$ variation. The theoretical drift mobility[63] for n-type GaAs doped at $10^{15} cm^{-3}$ would be approximately 7600 $cm^2 V^{-1} sec^{-1}$ at 300 °K. Both specimens are relatively free from ionized impurity scattering effects at temperatures above 150 °K. The data plotted in Figure 24 were corrected for the finite size of the ohmic contacts at the corners of the van der Pauw samples[64].

3.3 SCHOTTKY DIODE MEASUREMENTS

3.3.1 Diode Processing and Measurement Techniques

Gold Schottky diodes were formed on MBE layers grown on Te-, Si-, and Cr-doped substrates of GaAs. While plated gold was initially employed for the Schottky metallization where the underlying sybstrate was n^+- material,

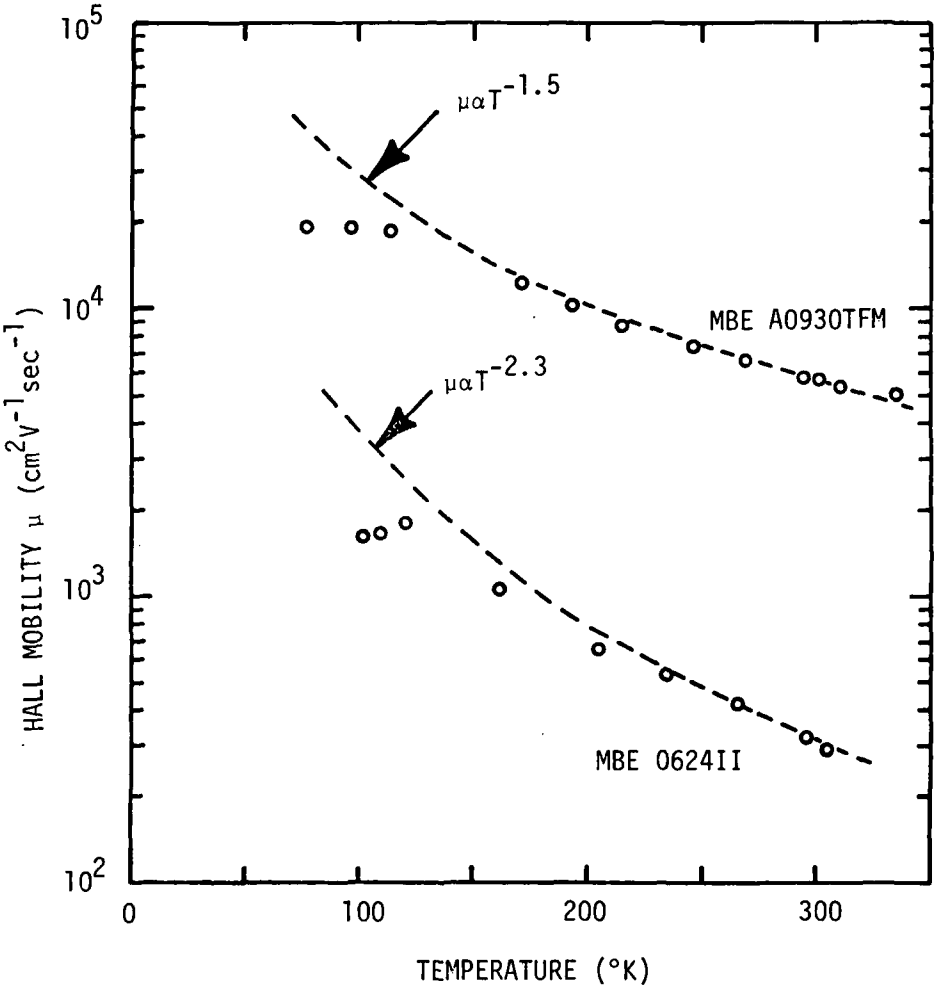


Figure 24. Temperature Dependence of Hall Mobility for GaAs Specimens Grown by MBE. MBE A0903TFM, n-type, 5.6 μm Thick. MBE 0624II, p-type, 1.2 μm Thick.

evaporated gold was used for most of the Schottky diodes. Photoresist techniques defined dots having a diameter of 254 μm (10 mils). Ohmic contacts (Ni/Au) were plated on the back surface of n^+-substrates. In the case of semi-insulating substrates, large area ohmic contact pads were first evaporated on the top surface of the epilayer. The deposition and alloying schedule for these contacts followed the same procedure used in preparing contacts for Hall samples (Section 3.2). The Schottky metallization was evaporated after the ohmic contact had been alloyed. Figure 25 shows the I-V characteristics measured for a 3.0 μm thick MBE layer A1006TFM grown on a Cr-doped substrate. The doping profile for this material is given in Figure 39 (page 92). Profiles for the epilayer beneath the Schottky diodes are derived by analyzing the diodes' C-V characteristics on a Materials Development Corporation Doping Profiler. The low leakage under reverse bias for layers processed in this manner, as Figure 25 indicates, allows accurate profiles to be measured. The reverse characteristic for MBE A1006TFM suggests a breakdown voltage slightly greater than 200 volts. Since the doping level is approximately $2 \times 10^{15} cm^{-3}$, this breakdown voltage compares favorably with the theoretical value of 220 V computed for abrupt GaAs junctions[65]. Thus the epilayer is free from the crystalline defects that lead to excessive current flow and premature breakdown.

3.3.2 Characteristics of Schottky Barriers Formed on MBE Layers

Experimental data are being collected as part of the study investigating interface characteristics of Schottky barrier diodes formed on MBE layers. Results comparing the surface doping concentration and zero bias capacitances for gold Schottky diodes on 22 GaAs layers deposited by chemical vapor deposition and 17 unintentionally doped GaAs layers grown by MBE are summarized below.

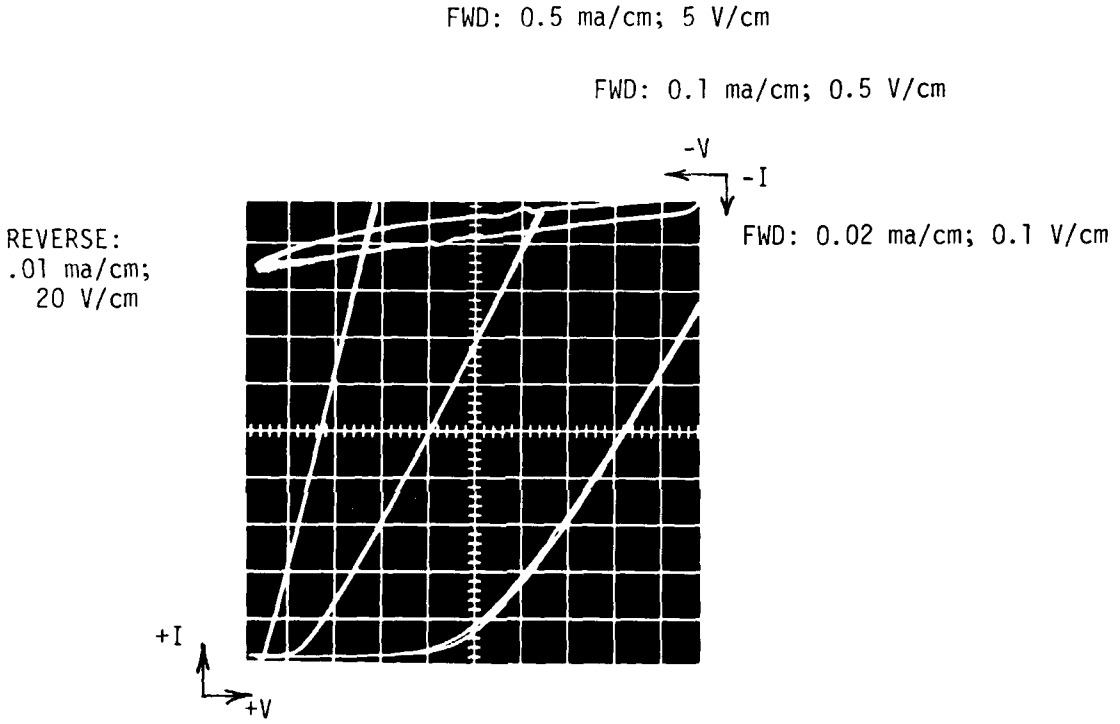


Figure 25. I-V Characteristics for a Gold Schottky Barrier Diode Formed on Layer MBE A1006TFM. The GaAs Epi-Layer was Grown on a Cr-Doped Substrate. The Diode Diameter was 254 μm (10 mils).

The capacitance per unit area at zero bias C_o/A for a Schottky diode is typically written as[66]

$$\frac{C_o}{A} = \left[\frac{q\epsilon_s N_d}{2(V_{bi} - kT/q)} \right]^{1/2} \tag{6}$$

where q = electronic charge,

ϵ_s = low frequency semiconductor dielectric constant,

N_d = donor density

V_{bi} = built-in voltage,

k = Boltzmann's contstant, and

T = junction temperature.

The build-in voltage can be obtained from

$$V_{bi} = \phi_{Bn} + \Delta\phi - (E_C - E_F) \tag{7}$$

where ϕ_{Bn} = height of metal-semiconductor barrier,

$\Delta\phi$ = image force barrier lowering,

E_C = energy of conduction band, and

E_F = Fermi level.

Gold on n-type GaAs yields a barrier height of 0.9 eV. The correction to V_{bi} due to $\Delta\phi$ is computed as [67]

$$\Delta\phi = \left[\frac{q^3 N_d (V_{bi} - kT/q)}{8 \pi^2 \epsilon_d^2 \epsilon_s} \right]^{1/4} \tag{8}$$

where ϵ_d = high frequency semiconductor dielectric constant.

Since the CVD layers were doped with sulfur, the donor energy level is located 0.006 eV below E_C. The activation energy for the unintentional n-type dopant in MBE layers has been measured to be 0.005 to 0.006 eV. Fermi-Dirac statistics

are used to solve for E_F in terms of N_d.

The above equations allow the zero bias capacitance to be calculated as a function of the doping concentration. A curve of this relationship is drawn as a solid line in Figure 26. Also plotted in the figure are the experimentally measured values of C_o and N_d obtained for CVD and MBE layers on the MDC Doping Profiler. The experimental data have been coded according to layer type and the diameter of the Schottky diodes. Prior to the evaporation of gold in an auxiliary vacuum system, the layers were washed in HCL and DI water. It can be seen that the experimental points cluster about the theoretical curve. The scatter is somewhat greater with the smaller diodes, but this hardly explains the MBE results. Indeed a more fundamental aspect appears to be operating for the latter.

The relationship given by Equation 6 is based upon a solution to Poisson's equation for a uniform doping distribution. A solution for a nonuniformly distributed dopant cannot generally be obtained in closed form. Insight into the presence or absence of a doping gradient at the interface can be derived from an analysis of a doping variation $N_d(x)$ of the form

$$N_d(x) = \alpha x^{\beta} \tag{9}$$

The width of the depletion layer W_o then becomes (Ref. 66, p. 135)

$$W_o = \left[\frac{\varepsilon_s(\beta+2)\ (V_{bi} - kT/q)}{q\alpha} \right]^{\frac{1}{\beta+2}} \tag{10}$$

Values of α and β have been computed using a least squares regression analysis to fit Equation 9 to 13 profiles free of surface leakage effects for the MBE diodes given in Figure 26. Both positive and negative quantities were obtained for β, and absolute β values fell in the range $0.12 \leq |\beta| \leq 4.27$

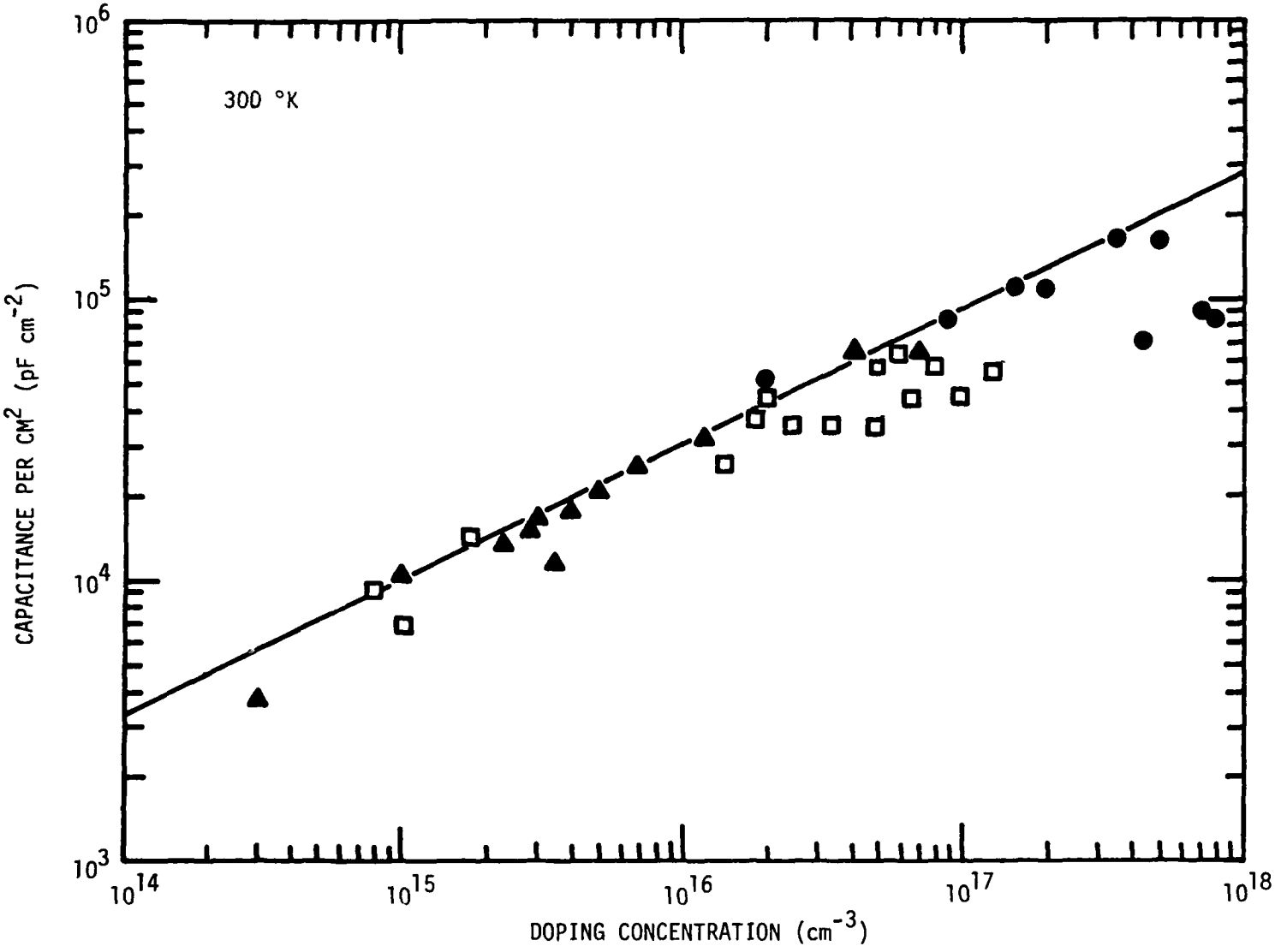


Figure 26. Theoretical (solid line) and Experimental Capacitances at Zero Bias for Gold Schottky Diodes on n-GaAs as a Function of Doping Concentration. Diode Diameters for CVD Layers are 3 mils (●) and 15 mils (▲); for MBE Layers 10 mil (□) Diodes were used.

which indicated that the unintentional doping at the interface was not uniform. Furthermore, when the computed values of α and β were combined with the depletion layer approximation $C/A = \varepsilon_s/W$ and the measured doping concentration at zero bias, the theoretical diode capacitances agreed on the average within 11 percent (standard deviation : eight percent) of the experimentally measured capacitances. Such agreement cannot be matched by attempting to fit the experimental data to the $\beta = 0$ curve in Figure 26. It is important to distinguish between the controlled doping in the CVD material and the relatively high, n-type background doping for certain deposition conditions and system modifications in the present MBE layers.

3.4 TRAP MEASUREMENTS

3.4.1 Instrumentation and Analytical Approach

Laboratory equipment has been assembled which detects the decay of deep level traps with a lock-in amplifier. The basic approach consists of charging traps during the on-portions of a train of 50 μsec pulses having a repetition rate lying in the 0.9 to 40 Hz region. The abrupt return to a reverse bias state (time constant of approximately 1.0 μsec for commercial instrumentation) allows the slower release of trapped charges from defects in the depleted layer to perturb the small signal, high frequency capacitance of a diode formed from the material under investigation. Changes in diode capacitance are detected by a capacitance meter (Boonton 72A) that is, in turn, connected to a lock-in amplifier (PAR 126). As the diode is swept in temperature, the response of the lock-in amplifier passes through a maximum at the point where the decay constant τ for a given trap level is uniquely related to the period of the applied pulse train[68].

A variable temperature probe stand was constructed to provide electrical

contact to gold Schottky diodes formed on the n-type MBE specimens. Temperature control was obtained by the convective transfer of heat between a flow of dry nitrogen gas and the specimen holder. To cool, the system is opened to the exhaust from a dewar of liquid nitrogen. For intermediate to high temperatures, the gas passes through a section of pipe wound with a nichrome heater. Important advantages provided by this approach include a high degree of electrical isolation between the heating circuit and the low-level, capacitance meter signals, a controlled environment around the test diodes, and rapid selective area probing over the sample.

The input tuned amplifier of the lock-in serves to pass only the fundamental Fourier component of the signal from the capacitance meter. If an exponential decay during period T is expanded in a Fourier series, the d.c. and fundamental frequency component can be written as[69]

$$f(t) = \frac{a_o}{2} + C_1 \sin\left(\frac{\pi t}{t_o} + \phi_1\right) \qquad (11)$$

where

$$C_1 = [\exp(-2t_o/\tau)-1] \,/\, [(t_o/\tau)^2 + \pi^2]^{1/2},$$

$$\phi_1 = \tan^{-1}(t_o/\tau\pi), \text{ and}$$

$$t_o = T/2.$$

The lock-in mixer passes f(t) for one half cycle and -f(t) for the next half cycle. A filter gives the time averaged response of the mixer output. If these operations are completed for f(t) given above, an expression is obtained for the output of the lock-in amplifier.

$$S = \frac{1}{2t_o}\left[\int_{-t_o}^{o} f(t)dt - \int_{o}^{t_o} f(t)dt\right], \qquad (12)$$

$$S = \frac{-2C_1}{\pi}\cos(\phi_1 + \varphi_a) \qquad (13)$$

where ϕ_a = adjustable phase of the lock-in amplifier.

A plot of this equation for $\phi_a = -\phi_1\ (\tau_{max})$ is given in Figure 27 as a function of a normalized decay constant $(\tau/\tau_{max} - \tau_{max}/\tau)$ where $\tau_{max} = 0.348497\ T$. A peak in signal amplitude is obtained at the temperature where $\tau = \tau_{max}$. The phase ϕ_1 of the input signal varies from 90° at high temperatures to 0° at the lowest temperatures. At the peak, ϕ_1 is 24.54569°.

Since the emission rates e_i corresponding to trap peaks are defined quantities,

$$e_i = \tau_i^{-1} = (0.3485\ T_i)^{-1}, \qquad (14)$$

they may be used in conjunction with the temperature measured at the peak maximum to fix the activation energy of the trap level. The parameters of interest follow directly from the standard emission equation

$$e = K\ T^2 \exp\ (-\Delta E/kT) \qquad (15)$$

where $K = \sigma\ v_{th}\ N_c\ T^{-2}$,

σ = capture cross section of the trap,

v_{th} = thermal velocity of carriers,

N_c = effective density of states in the conducting band,

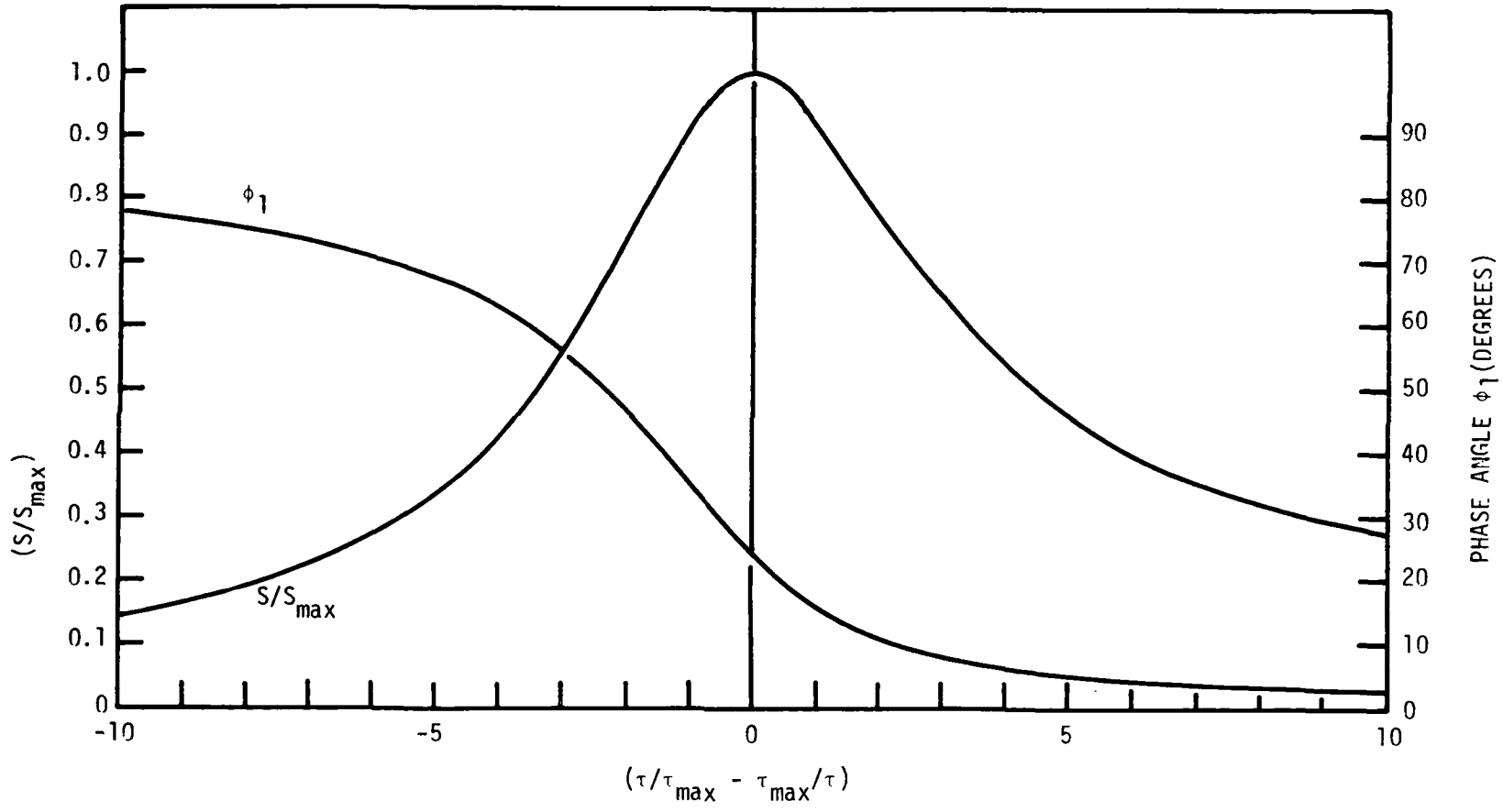


Figure 27. Theoretical Response of Normalized Signal Amplitude (S/S_{max}) for a Lock-in Amplifier Set to $-\phi_1(\tau_{max})$ During the Periodic, Exponential Emission of a Trap Level. A Peak is Observed when the Time Constant $\tau_{max} = 0.3485\ T$ where T is the Signal Period. The Variation in Signal Phase ϕ_1 is also shown over the same Interval of Normalized Time Constants.

ΔE = activation energy,

k = Boltzmann constant, and

T = temperature in °K.

Thus the slope of $\ln(\tau T^2)$ versus T^{-1} plot yields ΔE.

If the trap concentration N_t for a Schottky diode is much smaller than the majority carrier doping level N_d, then the concentration is simply related to the total change in capacitance ΔC measured after application of the bias voltage step[70]

$$\frac{N_t}{N_d} \simeq 2 \frac{\Delta C}{C_\infty} \tag{16}$$

where C_∞ is the capacitance under steady state bias conditions.

3.4.2 Deep Level Traps Observed in GaAs

Deep level traps have been observed in a number of GaAs specimens including not only MBE layers but also an implanted epilayer and a melt-grown specimen. The lock-in amplifier results reported below for the implanted layer are of special interest because they provide a comparison of trap measurements on the same piece of material by two independent laboratories using different techniques to sample the transient capacitance decay. This cross-check was valuable in establishing further confidence in the lock-in amplifier approach and the activation energies measured for traps found in MBE material.

The implanted layer 917-1 was grown in a CVD epi-reactor by Georgia Tech and subsequently implanted with Be by the Naval Research Laboratory. Two trap levels were identified by NRL[71] using a DLTS system containing a double boxcar for signal averaging[72].

A doping concentration profile for the 10 mil diameter, mesa diode tested on 917-1 is given in Figure 28. The steady state capacitance was established at a reverse bias potential of 5.0 volts. The depth and concentration corresponding to this bias are indicated directly on the profile.

Figure 29 presents the transient capacitance signals recorded for majority carrier pulses with a height of 5.0 volts and a width of 50 μsec. The peak heights indicate a defect density of $7 \times 10^{13} cm^{-3}$. As the frequency increases, the trap response shifts to higher temperatures. A replot of these data as shown in Figure 30 reveals an activation energy of 0.61 eV. The double boxcar method predicted $\Delta E = 0.58$ eV[71]. This agreement is judged to be a satisfactory test of the two DLTS techniques.

The vertical translation of the curves shown in Figure 30 suggest a different capture cross section is being observed by the two experimental techniques. The following formula is obtained for the apparent capture cross section of electrons in GaAs

$$\sigma_n = 4.519 \times 10^{-21} \, eT^2 \exp(\Delta E/kT) \qquad (17)$$

if an effective mass of 0.068 m_o is substituted into the conventional definitions of v_{th} and N_c (Ref. 66, pp. 4,26). Capture cross sections of $2.3 \times 10^{-14} cm^2$ and $1.3 \times 10^{-13} cm^2$ are computed for the double boxcar and lock-in amplifier data, respectively. Vertically translated e(T) curves with essentially similar slopes have been observed for GaAs by other workers[73]. The question remains open of whether the present differences are derived from fundamental features of the measuring techniques or from slightly modified properties of junctions formed at different positions on the implanted epilayer

Different activation energies were measured by the double boxcar and the lock-in amplifier for minority carrier injection pulses. As Figure 31 indicates,

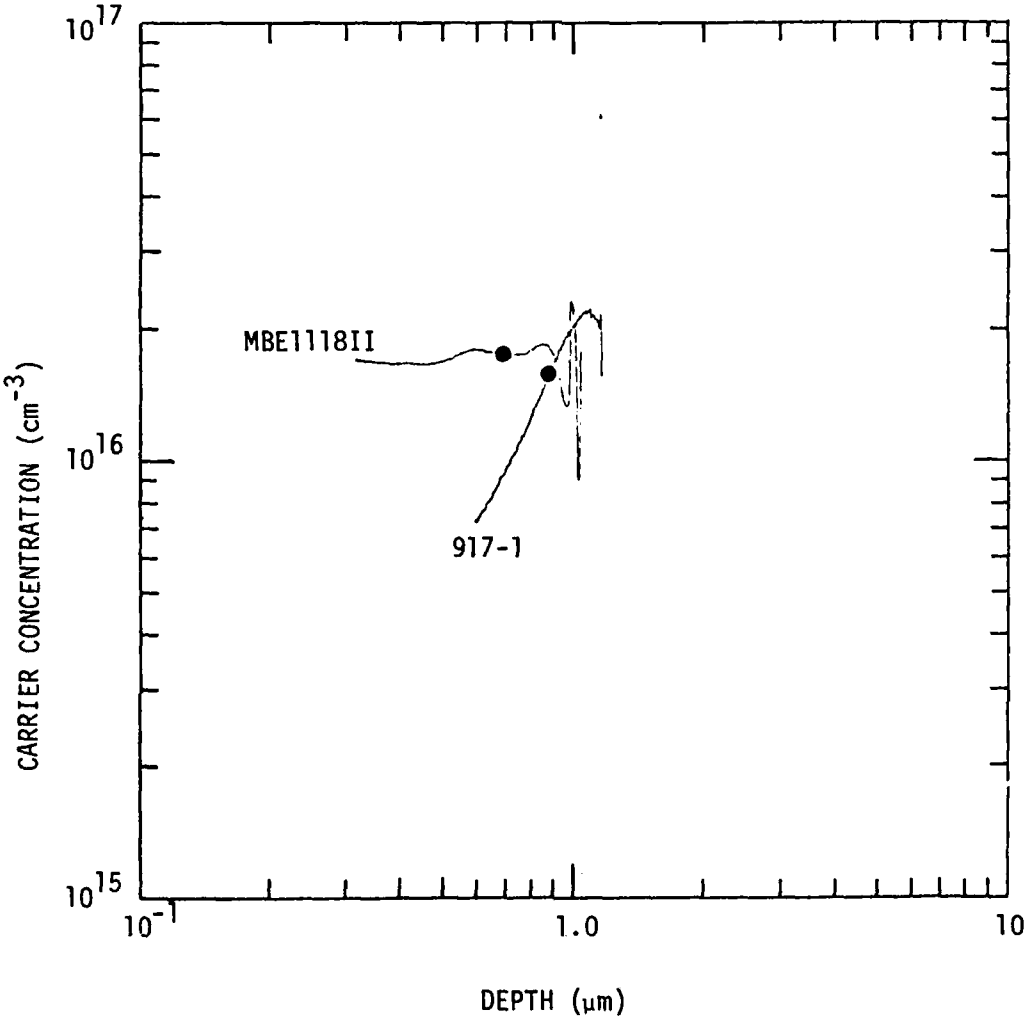


Figure 28. Doping Concentration Profiles for a p-n Junction Diode Formed on a Be Implanted CVD Layer 917-1 and a Au Schottky Diode Formed on Layer MBE1118II. Dots on Each Profile Correspond to the Reverse Bias Potential of 5V which Established the Quiescent Capacitance.

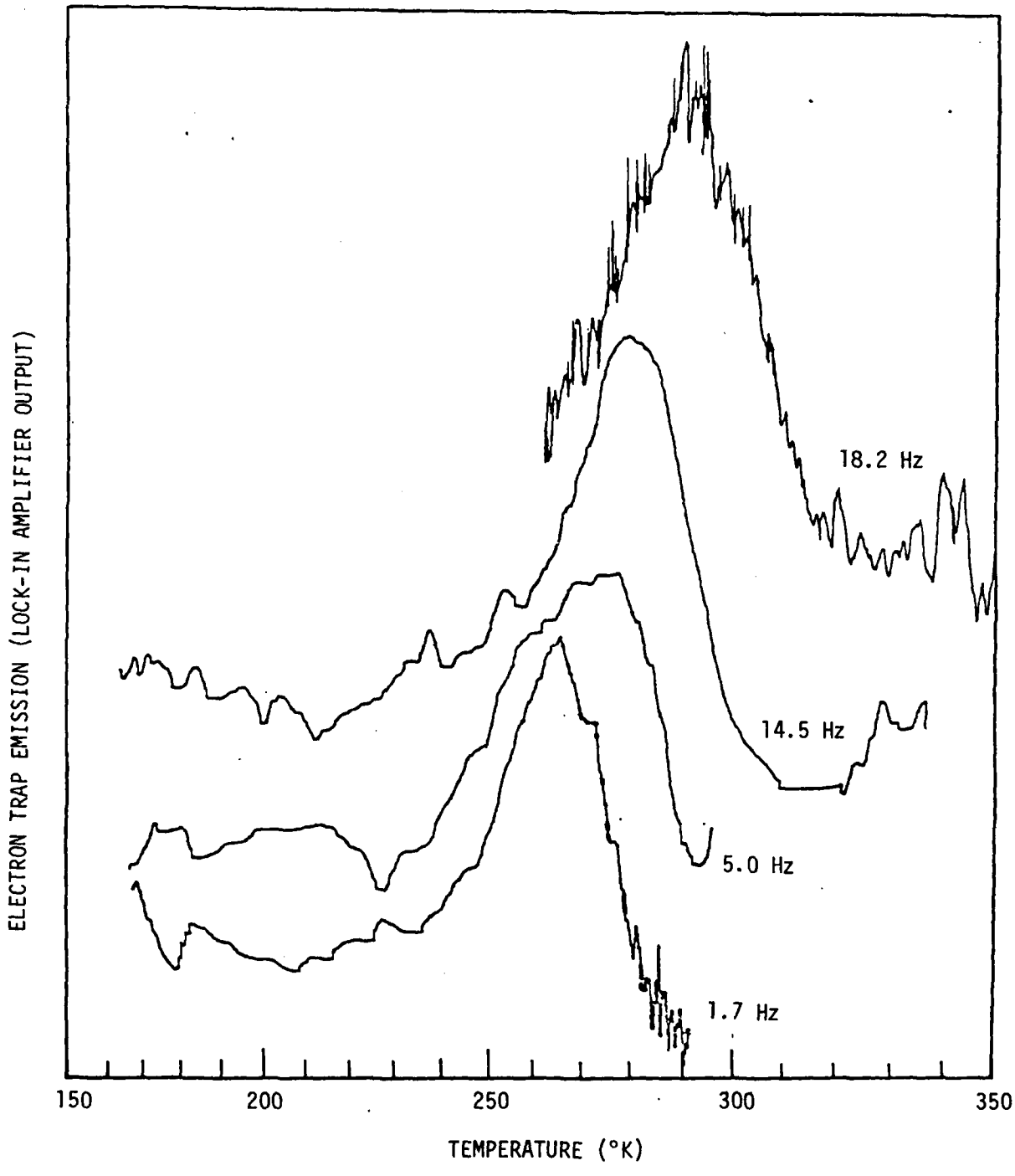
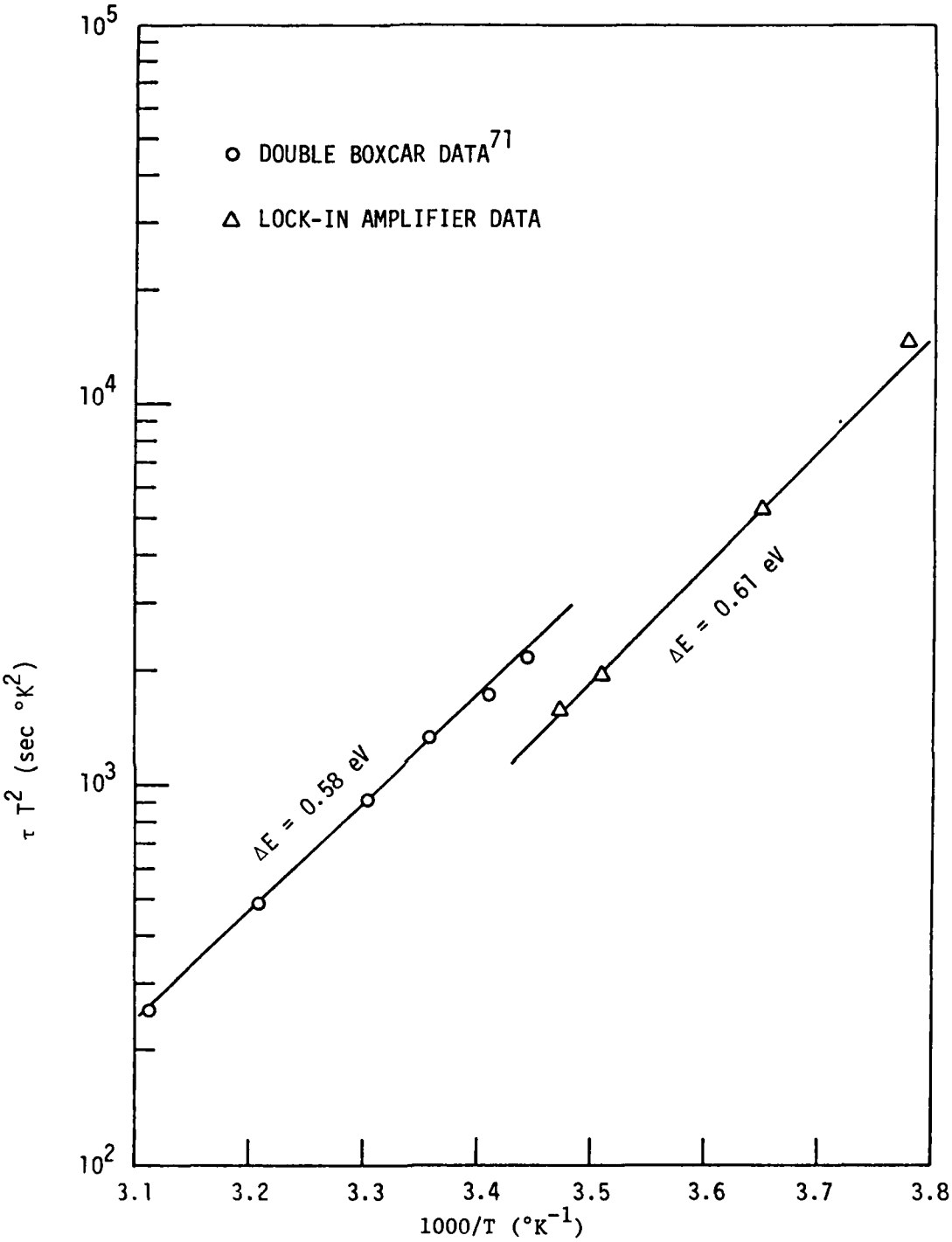


Figure 29. Spectra of Majority Carrier Trap Emission in Be Implanted GaAs No. 917-1. The Frequency of the 50 μsec Saturating Pulse is Indicated on Each Trace.



Determination of the Activation Energy for Majority Carrier Traps in Implanted GaAs No. 917-1. The Data were Derived from Measurements of the Temperature Dependence of Transient Capacitance Transients. The Results Compare Two Signal Processing Tech-

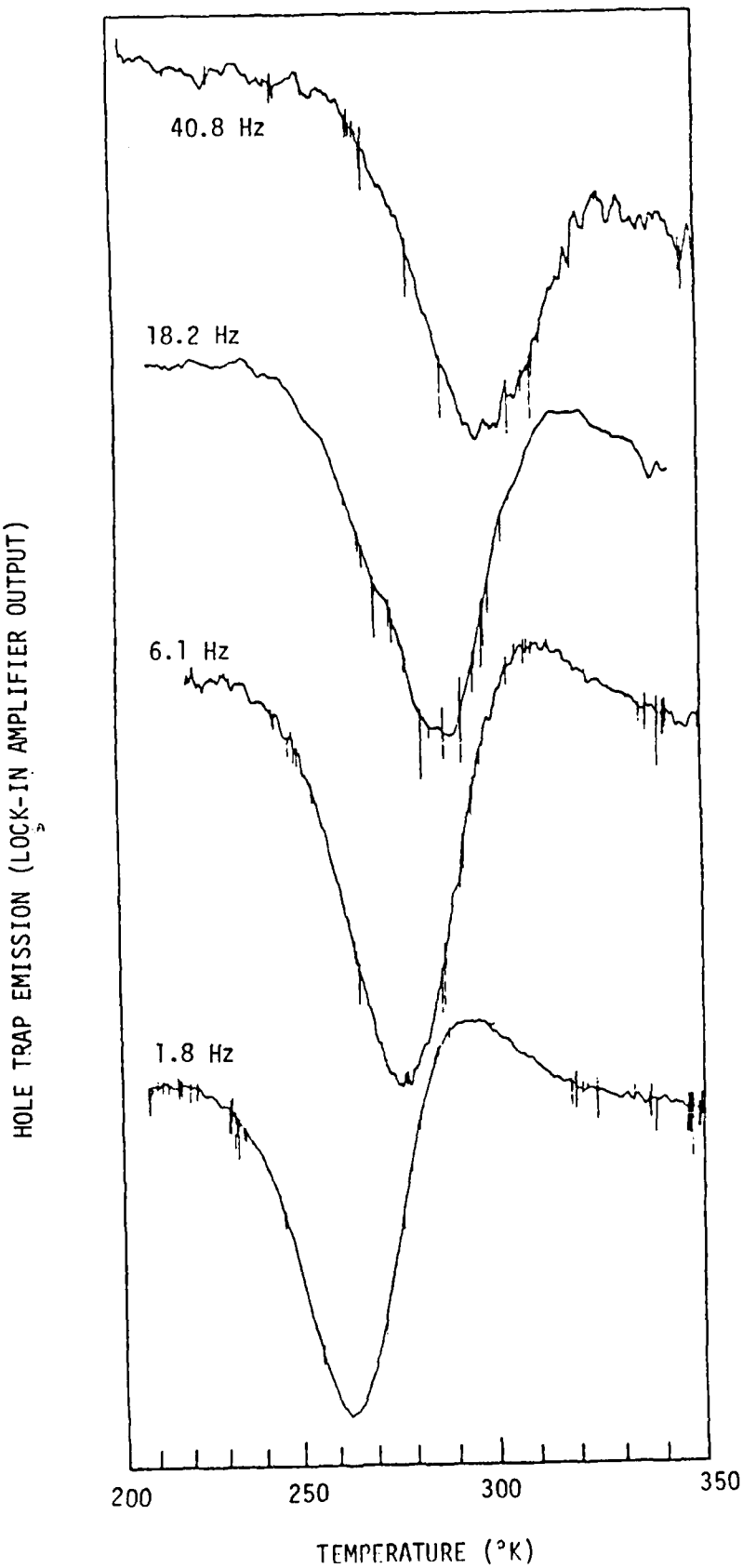


Figure 31. Spectra of Minority Carrier Trap Emission in Be-Implanted GaAs No. 917-1. The Frequency of the 50 μsec Injection Pulse is Indicated on Each Trace.

the lock-in amplifier predicts trap peak positions that are similar to those found for majority carriers. Results for the double boxcar at comparable rate windows showed minority carrier peaks occurring higher in temperature with $\Delta E = 0.75$ eV. This discrepancy is not understood and a better characterization of the experimental conditions is in order for junctions operating under minority carrier injection.

Deep level majority carrier traps were found for the MBE layer 111811 characterized in the doping profiles in Figure 28 (p.68). The traps were observed in the 150 to 300 °K range for rate windows for 5.1 to 51 sec^{-1}. The central peak shown in the spectra of Figure 32 has an activation energy of 0.36 eV and a measured density of 3×10^{13} cm^{-3}. A second majority carrier trap level is just resolved at the frequencies of 17.2 and 5.1 Hz. The activation energy of this level is estimated to be approximately 0.2 eV.

Deep level trap spectra for melt-grown GaAs[74] and several other MBE layers are presented in Figure 33. Figure 34 shows the doping profiles for these specimens. Additional growth details and trap data are summarized in Table 2. It can be seen in Figure 33 that the position of the spectral peak gives only a general indication of the activation energy ΔE. Improved accuracy results by correlating the shift in spectral peaks with different pulse periods or rate windows[76]. This approach was followed in compiling most of the ΔE values in Table 2. In the case of MBE A1216, the activation energy was estimated using the approximate expression $\Delta E \sim 23.7$ kT where T(°K) is the DLTS peak position[55].

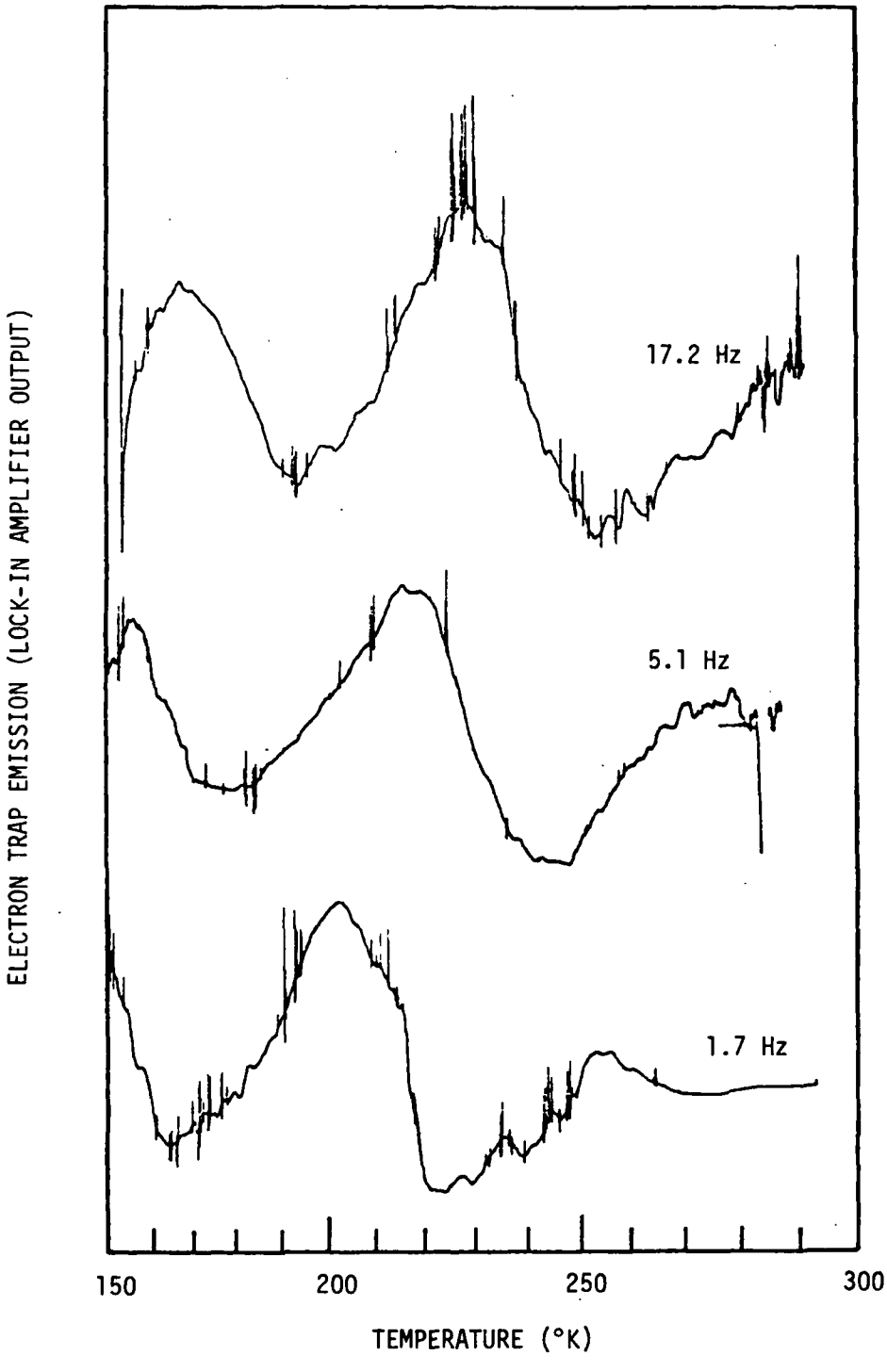


Figure 32. Spectra of Majority Carrier Trap Emission in GaAs MBE 1118II. The Frequency of the 50 μsec Saturating Pulse is Indicated on Each Trace.

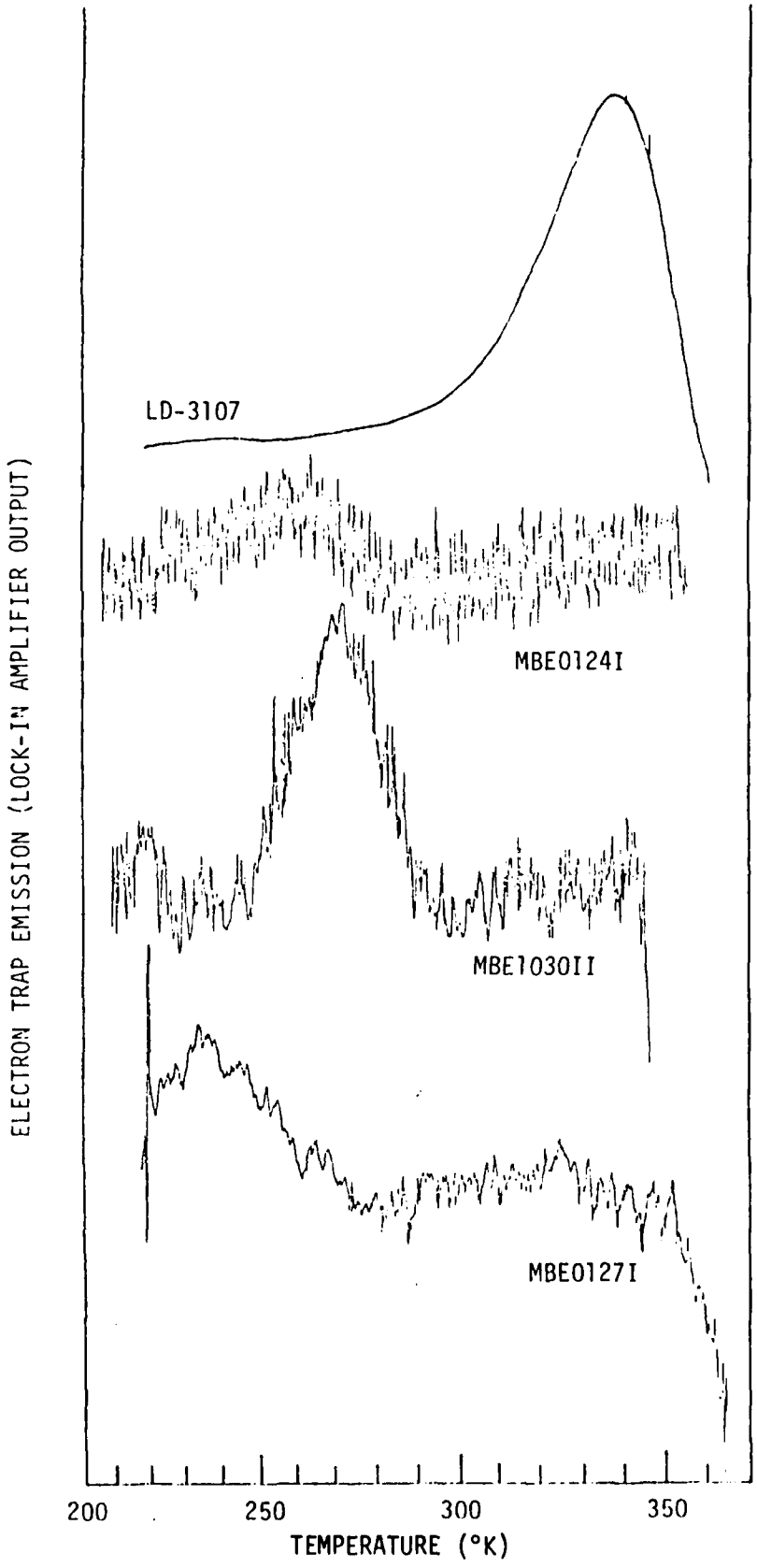


Figure 33. Trap Spectra for a GaAs Bulk Specimen and Three MBE Layers. The Frequency of the Saturating Pulse is 1.7 Hz for Each Trace.

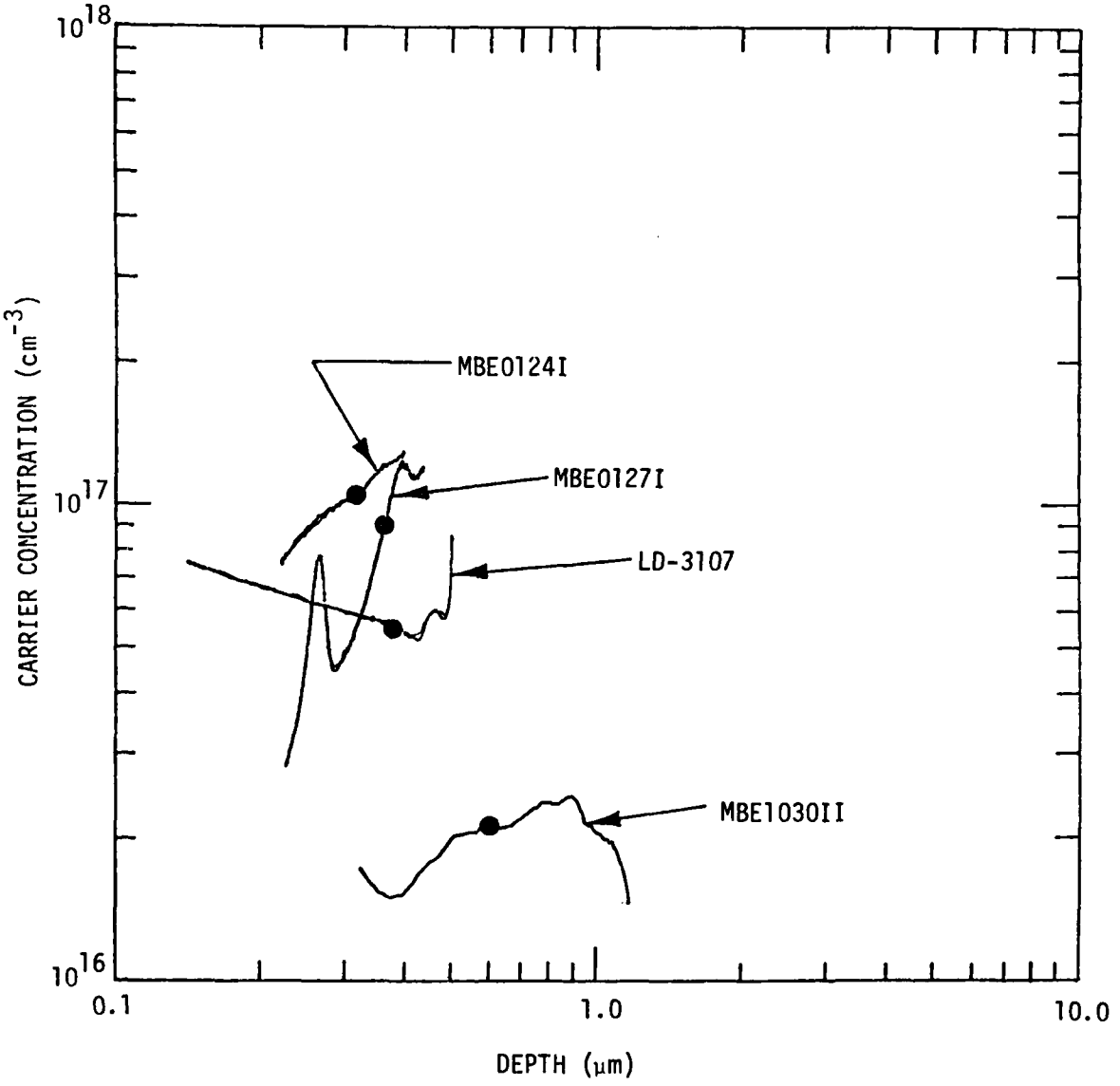


Figure 34. Doping Concentration Profiles Using Au Schottky Diodes Formed on a GaAs Bulk Specimen and Three MBE Layers. Dots on Each Profile Correspond to the Reverse Bias Potential which Established the Quiescent Capacitance for Trap Studies.

Table 2. Summary of Trap Data for Unintentionally Doped n-type GaAs Specimens. The Deposition Rate for MBE Layers was 0.9 to 1.0 μm/hr.

Specimen	$T_{substrate}$ During Growth (°C)	Reverse Bias (V)	Observed Activation Energy (eV)	Trap Concentration (cm^{-3})
LD-3107	*	5.0	0.83	2×10^{14}
MBE1030II	597	4.0	0.72	9×10^{13}
MBE1118II	580	5.0	0.36	3×10^{13}
MBE0124I	515	4.0	0.72	3×10^{14}
MBE0127I	514	4.0	0.38	3×10^{14}
MBEA1216[75]	600	2.0	0.24,0.35,0.46	*

As indicated in Figure 33, the dominant trap level for unintentionally doped, bulk GaAs is a deep lying level with an observed activation energy of 0.83 eV. This figure agrees with the level at 0.83 eV (ΔE_{meas} - 2kT) that has been associated with an O center[76]. It is interesting that the dominant trap levels for n-type MBE material grown under As-stabilized conditions are quite different from the defect level found for melt-grown GaAs.

Another significant feature of the present results is that the deep traps for unintentionally doped MBE layers 1030II, 1118II, 0124I, and 0127I grown with the BeO substrate heater do not occur at the same activation energies as those reported for Si, Sn, and Ge doped MBE layers[55] although the relative trap concentrations and doping levels are comparable

in magnitude. The levels for layers grown on the BeO heaters are more like E3 (0.41 eV) and E4 (0.71 eV) found in electron-irradiated n-GaAs[77]. In view of the sensitivity of ΔE to systematic temperature errors as described previously for the O defect[76] where ΔE ranged between 0.75 and 0.83 eV, it is, of course, possible that the trap levels given in Table 2 really correspond to levels such as M3, M4, or M5 with energies of 0.30, 0.48, or 0.58, respectively[55]. Since good agreement was obtained for majority carrier traps in the implanted layer 917-1 and the melt-grown GaAs specimen LD-3107, this hypothesis is not entirely satisfactory. The traps observed in A1216 grown on the large fused quartz substrate heater show a closer correspondence to the M1, M3, and M4 levels reported for Si-doped MBE layers[55]. As discussed in Section 4.2.2, other data indicate that Si was the unintentional donor in A1216.

Differences in deep level traps in MBE material are observed for different system configurations. Two possible interpretations are suggested. First, contaminants lodged in the relatively porous BeO (which was chemically cleaned after each run) may be available for incorporation during the epilayer growth. Similar trap energies and higher concentrations are observed for layers grown at lower substrate temperatures. An increase in sticking coefficient for the dopant species would explain this behavior. While the active donor level is quite shallow (Section 4.2.1) with respect to the trap levels (in fact, the activation energy of the donor of 0.006 eV represents the absolute minimum energy detectable by the DLTS method), a defect complex associated with chemical impurity incorporation could lead to the observed deep level states. Another interpretation hinges on the improved knowledge of the substrate temperature available with the fused

quartz heater. The DLTS spectra for layers grown on the BeO heaters could be dominated by non-stoichiometric defects associated with significant differences between the indicated and actual growth temperatures.

3.5 SPECTRAL PHOTOLUMINESCENCE MEASUREMENTS

Spectral photoluminescence techniques offer simplicity, versatility and precision in identifying trace impurities and defects. The usefulness of photoluminescence has been enhanced with the availability of published data on optical transitions associated with shallow dopants and native defects[78-83]. Initial photoluminescence studies of MBE GaAs were taken on relatively highly doped specimens at temperatures of 77-300 °K with spectrometers of limited resolution[15,15,58,84,85]. Little attention has been directed toward resolving structural details in the exciton region using lightly doped specimens, spectrometers with high resolution, and low temperatures ($\leq$ 4.2 °K)[20,86].

One of the first observations of a number of discrete, partially resolved lines in the exciton region was obtained on the unintentionally doped layer MBE A1216 grown with the large fused quartz substrate heater. Spectra taken at NRL[87] are presented in Figure 35. Similar spectra were obtained on this sample at Air Force Avionics Laboratory[88], Wright Patterson Air Force Base and Royal Signals and Radar Establishment[89], Malvern, England. The detailed structure in the exciton region indicates that the layer quality is approaching that observed in undoped VPE GaAs[90]. The line at 1.5148 eV occurs at the n = 1 state of the free exciton. A line associated with an exciton bound to a neutral donor is identified at 1.5140 eV, and there is evidence of an unresolved donor state at 1.5112 eV. The breadth of the lines in this sample do not allow a unique assignment of chemical shifts for a

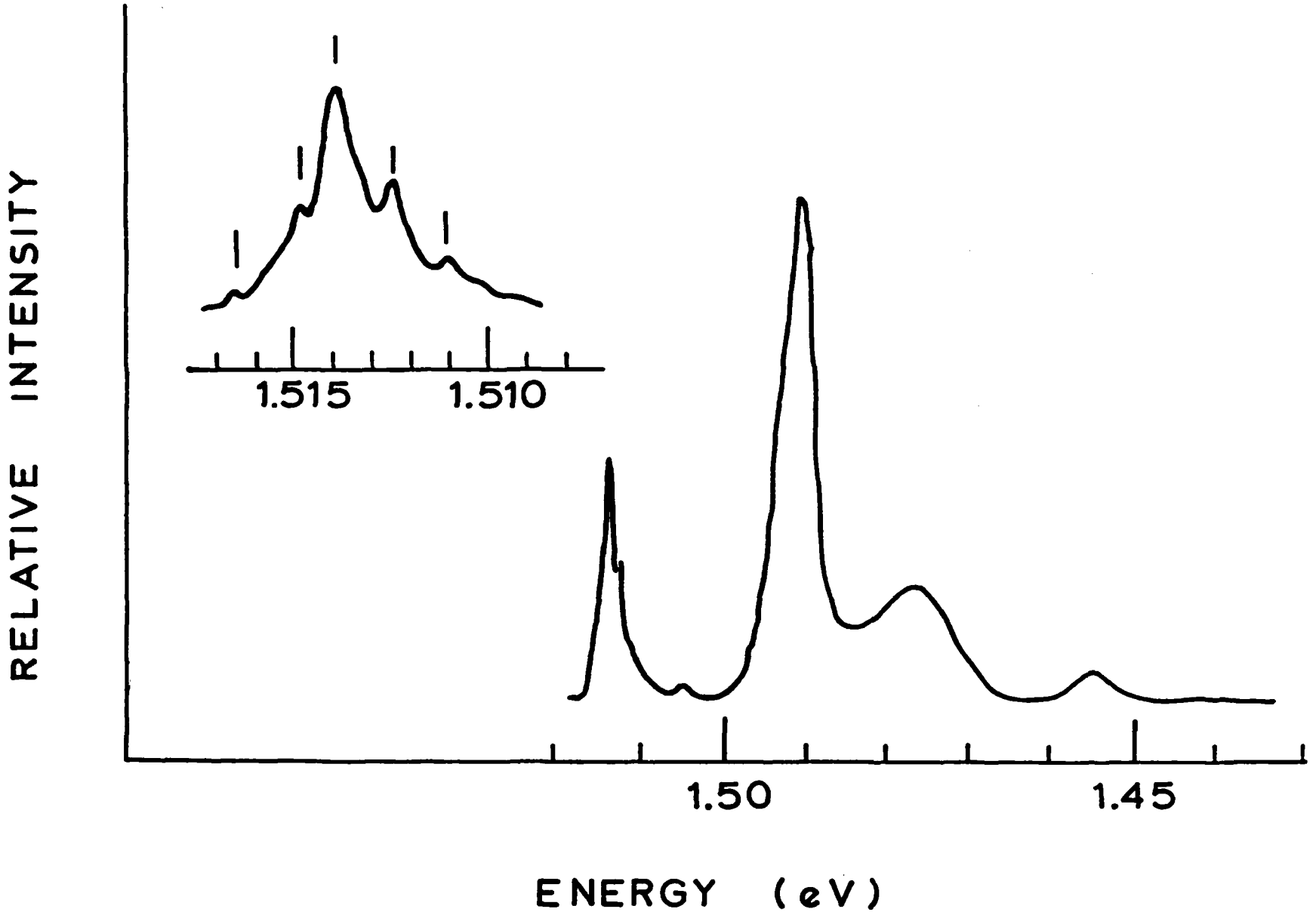


Figure 35. Photoluminescence Spectra Measured at 4.2 °K on MBE A1216. The Inset Shows Band Structure in the Exciton Region.

particular donor to be drawn from the data. In the free to bound acceptor region bands with binding energies of 0.0286 eV and 0.0426 eV lie close to the binding energies reported for C and Ge, respectively in GaAs[80]. Carbon is frequently reported in GaAs grown by MBE, CVD and LPE. The Ge line is quite puzzling, however, since there is no record of Ge in the vacuum system. A recent survey of photoluminescence characteristics of MBE layers grown by four independent laboratories further confirms the presence of carbon at 1.493 eV[91].

4.0 UNINTENTIONAL BACKGROUND DOPING INVESTIGATION

4.1 INTRODUCTION

The precise control over film thickness, surface smoothness and doping profiles afforded by MBE makes it a particularly attractive choice for growing high frequency FET material. High performance FETs do require, however, thin electrically active regions free from defects and diffusion products associated with the initial deposition on the semi-insulating substrate. In one approach to this materials problem, a high resistivity buffer layer is formed between the FET and the substrate. A number of experiments were defined to investigate the properties of unintentionally doped MBE layers for buffer applications. The results of these experiments are described in this section.

Before discussing the individual experiments, it is instructive to note that the background doping of the buffer layer should be $10^{14}cm^{-3}$ or less. Three practical difficulties are encountered in experimental analysis of buffer layer material. First, the background measurement for micron thick buffer layers on a GaAs substrate demands a sensitivity of approximately one part in 10^9. Such a sensitivity exceeds the detection limits of conventional spectroscopic techniques such as Auger, EDXA, electron microprobe, and neutron activation. Although high resolution photoluminescence provides spectroscopic information, particularly for shallow levels in GaAs, it has only recently been shown that high resolution photoluminescence can be successfully applied to MBE layers. Free-to-bound transitions have been associated with C, Ge, Mn, and Si in lightly doped MBE specimens[20,86,91]. Hall measurements provide adequate

sensitivity. Unfortunately, they cannot generally identify a particular doping species because of the limited concentration range over which a particular dopant source is active. Secondly, doping profiles constructed from C-V measurements of Schottky diodes become tenuous at low concentrations since the built-in voltage decreases as the Fermi-level approaches the mid-gap position. Finally, experience indicates that system modifications and differences in growth techniques can have a significant impact on the background doping. Several growth runs in conjunction with controlled substitutions are necessary to establish the background for a particular system configuration and operating schedule. Runs, therefore, tend to group in series punctuated by general system clean-ups including high temperature outgassing of the sources (>1200 °C for 30 minutes) and fresh loads of Ga and As.

4.2 UNINTENTIONAL n-TYPE DOPANTS

4.2.1 Growth on BeO Substrate Heaters

Electrical characterizations have been completed for approximately 30 GaAs layers prepared by MBE using BeO plates carrying sputtered Ta resistive heaters. The data have been correlated with the various system parameters that influence the electrical properties of the epitaxial layers. It was recognized that multiple doping sources could be competing for dominance with any given set of system components and deposition sequence. The evidence indicates that BeO substrate heaters contribute a background donor with a density falling in the mid $10^{16}cm^{-3}$ range. Support for this conclusion is set forth below.

The dominant doping was n-type. Only five layers in the group were p-type and these were traced to abnormal conditions in the system associated with hot stainless steel (Section 4.3.1). Table 3 summarizes the principal deposition parameters and doping concentrations for twenty-one n-type layers with

Table 3. Characteristics of Unintentionally Doped, n-type GaAs Layers Grown by MBE on Te-doped Substrates Attached to BeO Substrate Heaters. Concentration Data were Derived from Profile Measurements Using Au Schottky Diodes (10 mils dia.).

MBE Layer	Vacuum Exposure Before Growth (hr)	Thickness (μm)	Growth Rate (μm hr)	$T_{Substrate}$ (°C)	Concentration (cm^{-3})
1030II	14.0	1.0	1.0	597	2×10^{16}
1116II	18.5	1.0	0.5	565	$<2 \times 10^{15}$(PT)
1118I	42.5	0.9	0.9	540	$<1 \times 10^{16}$(PT)
1118II	40.5	1.0	1.0	580	1×10^{16}
1130III	144.0	3.2	0.9	575	7×10^{14}
0120II	17.5	2.0	0.9	515	7×10^{16}
0124I	69.0	>0.4	>0.2	515	1×10^{17}
0125II	85.0	2.0	0.9	515	1×10^{17}
0127I	16.0	1.8	0.9	515	5×10^{16}
0225II	4.9	3.7	1.8	560	5×10^{16}
0414II*	17.0	0.9	0.3	575	$<2 \times 10^{16}$(PT)
0415I*	37.0	0.7	0.2	600	6×10^{16}
0419I*	22.5	0.9	0.3	580	2×10^{16}
0420II	43.5	0.6	0.2	600	$<1 \times 10^{16}$(PT)
0422II	5.2	0.7	0.2	600	8×10^{16}
0426II*	26.0	1.1	0.3	600	8×10^{15}
0503II	4.3	0.7	0.2	600	3×10^{16}
0520I	17.0	>0.3	>0.2	600	2×10^{17}
0524III	27.0	>0.6	>0.3	580	7×10^{16}
0525I	43.5	1.0	0.7	600	3×10^{16}
0525II*†	44.0	0.3	0.2	580	6×10^{16}

PT = Punched Through

* Doping Concentration Substantiated with Hall Data for Concurrent Deposition on Cr-doped Substrate

† Cr-doped Substrate

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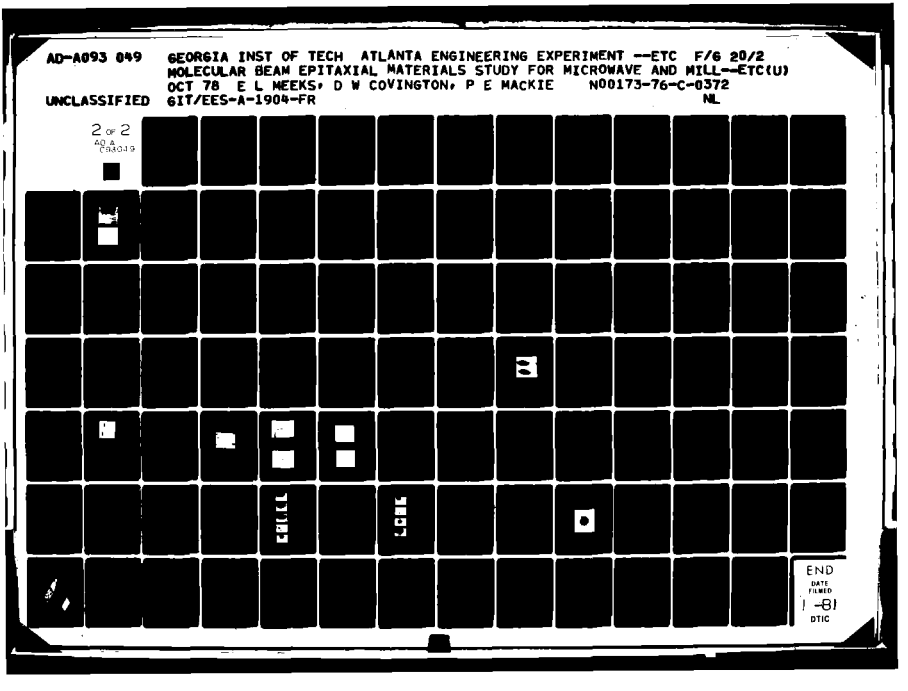


reasonably uniform doping profiles. The average concentration for the layers that were not punched through is $5.6 \times 10^{16} cm^{-3}$. Doping concentrations were taken from C-V data of Au Schottky diodes evaporated on the MBE layer. As the table indicates, autodoping from the substrate is not a factor at these concentrations and growth temperatures. Careful examination of Table 3 reveals that pumping for a longer period of time tends to yield a slightly lower background doping level for a given substrate temperature range. Increasing the substrate temperature also tends to give a lower background doping for a given vacuum exposure. The depositions at 515 °C employed two BeO elements, a carrier plate in conjunction with the main heating element. Several other experiments were conducted to further probe the source and deposition characteristics of the n-type dopant.

Observing carbon grow on freshly cleaned GaAs surfaces in a vacuum environment prompted a series of runs which emphasized a rapid pumpdown to the 10^{-9} Torr range. Depositions for these runs began approximately five hours following a system load. Figure 36 gives doping profiles for three specimens deposited under these conditions. Background pressures before oven heating were 3.4×10^{-9}, 5.7×10^{-9} and 8×10^{-9} Torr for MBE0225II, 0422II, and 0503II, respectively. Other deposition parameters are listed in Table 3. Since lower doping is obtained for layers exposed to considerably longer predeposition vacuum conditions, it is concluded that surface carbon is not a constraint on background doping at $10^{16} cm^{-3}$ levels.

The possibility has also been eliminated that the doping arose from either the steel carriage assembly supporting the substrate heater or from the clip attached to the front surface of the substrates during some runs. No improvement in doping level was obtained in the last four entries in Table 3 which were grown with an open carriage assembly having an improved UHV

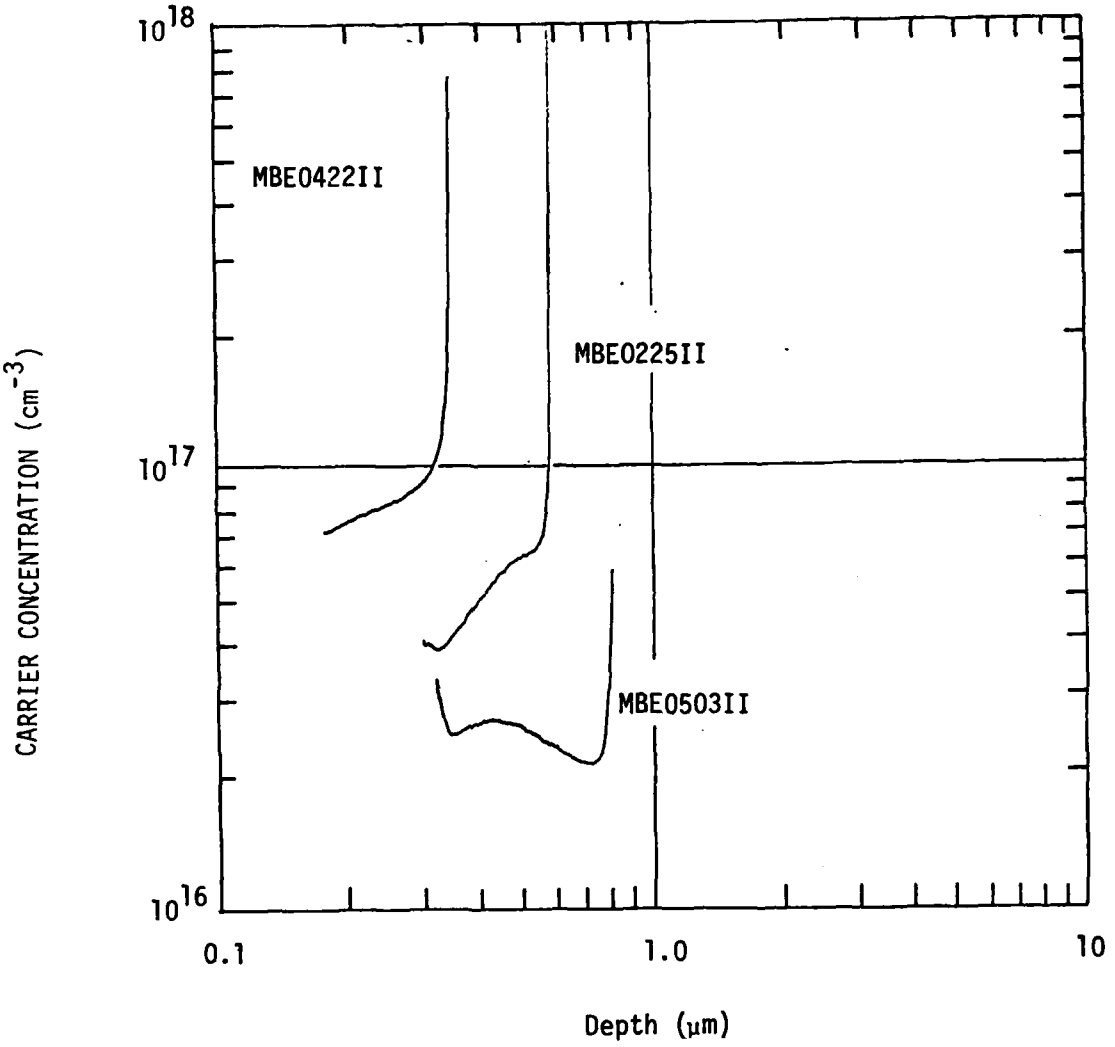


Figure 36. Background Doping Concentration Profiles for Three MBE GaAs Layers Grown Under Conditions Which Minimized in situ Carbon Deposition.

compatibility. A theoretical estimate for the mean distance over which an adatom could diffuse[92] indicates that for jump distances between adsorption sites on the GaAs surface of atomic dimensions and a substrate temperature of 580 °C, then planar doping regions tens of mils in extent could accompany impurity adatom desorption energies of the order of 2.7 eV. A systematic survey of the region adjacent to a stainless mounting clip was conducted for MBE 0419I. An array of 50 Au dots each 10 mils in diameter was formed on the specimen. The array was surrounded by a large area Schottky diode. A map of the reverse bias voltage at one ma and the zero bias capacitance is shown in Figure 37. Standard deviations from the mean values of 32.21 pF and 15.13 V are 1.78 pF and 1.36 V, respectively. The geometrical distribution of C_0 and V_B argues against the association of the clip with localized contributions to the unintentional background doping level (low $10^{16} cm^{-3}$).

Table 4 correlated deposition conditions and background doping concentrations with four other system parameters; namely, high temperature outgas of the source ovens in a separate UHV chamber, operation with 6N As load, operation with a cold trap, and substitution of an alternative dielectric for the BeO heater. While the first three parameters have little impact on the background doping, a striking drop in carrier concentration and a switch in carrier type is observed when fused quartz or boron nitride was substituted for the BeO. When BeO was reintroduced in the run series (MBE0610I), the carrier type reverted to n-type and the doping level increased. The single n-type layer with a fused quartz heater, MBE0615I, was the first to be grown with the cold trap in operation. An increase in nitrogen comparable with the residual water vapor complex was observed with the RGA on this run during refills of the cold trap. After tightening the tubing interconnections, the leak was eliminated and the growth again became p-type.

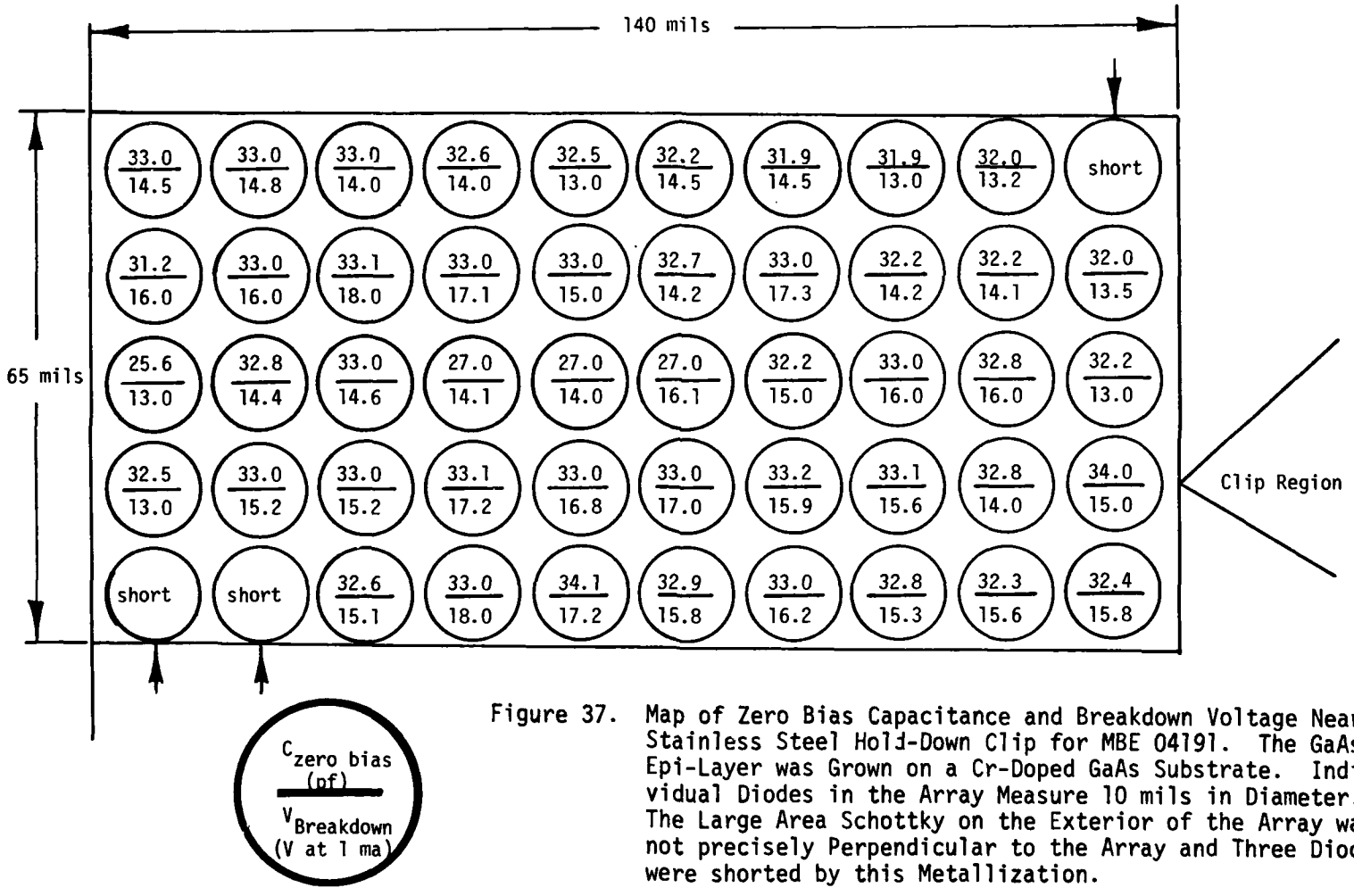


Figure 37. Map of Zero Bias Capacitance and Breakdown Voltage Near Stainless Steel Hold-Down Clip for MBE 04191. The GaAs Epi-Layer was Grown on a Cr-Doped GaAs Substrate. Individual Diodes in the Array Measure 10 mils in Diameter. The Large Area Schottky on the Exterior of the Array was not precisely Perpendicular to the Array and Three Diodes were shorted by this Metallization.

Table 4. Summary of Deposition Parameters, Doping Concentration, and System Parameters Varied During Background Doping Studies of n-type GaAs Grown by MBE on Cr-Doped Substrates

	DEPOSITION PARAMETERS				DOPING (296 °K)		SYSTEM PARAMETERS			
MBE Layer	Vacuum Exposure Before Growth (hr.)	Thickness (μm)	Growth Rate (μm/hr)	$T_{Substrate}$ (°C)	Carrier Type	Concentration (cm^{-3})	Oven Outgas (°C)	As Source Purity	Cold Trap Operating	Substrate Heater Type
04141I	17.0	0.9	0.3	575	n	2×10^{16}	1090	5N	no	BeO
0419I	22.5	0.9	0.3	580	n	2×10^{16}	1090	5N	no	BeO
0525II	44.0	0.3	0.2	580	n	6×10^{16}	1090	5N	no	BeO
0603I	39.5	1.7	0.4	620	p	2×10^{15}	1200	6N	no	FQ
0607III	17.5	1.6	0.4	640	p	5×10^{15}	1200	6N	no	FQ
0610I	16.5	1.4	0.3	580	n	1×10^{16}	1280	6N	no	BeO
0615I	20.0	0.5	0.3	580	n	5×10^{16}	1280	6N	yes*	FQ
0620I	68.0	1.3	0.6	580	p	6×10^{15}	1280	6N	yes	FQ
0624II	23.0	1.2	0.6	600	p	7×10^{15}	1280	6N	yes	FQ
0817II	23.5	1.2	0.4	585	p	8×10^{15}	1233	6N	yes	PBN

FQ = Fused Quartz
PBN = Pyrolytic Boron Nitride
Concentrations taken from Hall measurements and profiles using Schottky barrier diodes
* Small N_2 leak during trap refills

The activation energy of the unintentional n-type dopant was taken from Hall data on van der Pauw specimens of layers MBE0419I and MBE0525II shown in Tables 3 and 4. The temperature variation of the Hall coefficient R and resistivity ρ are given in Figure 38. The low temperature saturation in R likely signals the onset of impurity band conduction. Nearer room temperature the weak dependence of R upon T^{-1} indicates the shallow doping in these specimens. Detailed curve fitting[93] of the data in Figure 38 for an acceptor compensation $N_A = 0.25\ N_D$ yields an activation energy of 0.005 eV for MBE0419I and 0.006 eV for MBE0525II. The restricted temperature range limits the accuracy in assigning these values to approximately 0.002 eV. Within these limits the similarity between the activation energies for the two samples allows the conclusion to be drawn that the same dopant is operative for growth in the old (MBE0419I) and open (MBE0525II) carriage assemblies. The room temperature values of ionized donor concentrations agreed within 25 percent of the average doping level read from doping profiles determined with Schottky barrier diodes. The variation in scattering factor r with scattering type and temperature was neglected and a constant value of unity was employed in the above calculations. The Hall mobility $\mu = R/\rho$ may be readily obtained from the data in Figure 38. The sample with the higher mobility MBE0525II was 0.3 μm thick. The room temperature mobility of 3140 $cm^2\ volt^{-1}sec^{-1}$ compares favorably with the figure of 3930 $cm^2\ volt^{-1}sec^{-1}$ estimated for Sn-doped MBE layers of similar thickness and doping level ($1 \times 10^{17} cm^3$) on chemically etched, Cr-doped GaAs[31].

In summary, the above analyses link an unintentional n-type dopant in GaAs layers with the use of BeO substrate heaters. As Table 3 indicates, the doping concentration falls in the mid $10^{16} cm^{-3}$ range. These data also show that the unintentional doping is not characterized by a single process such

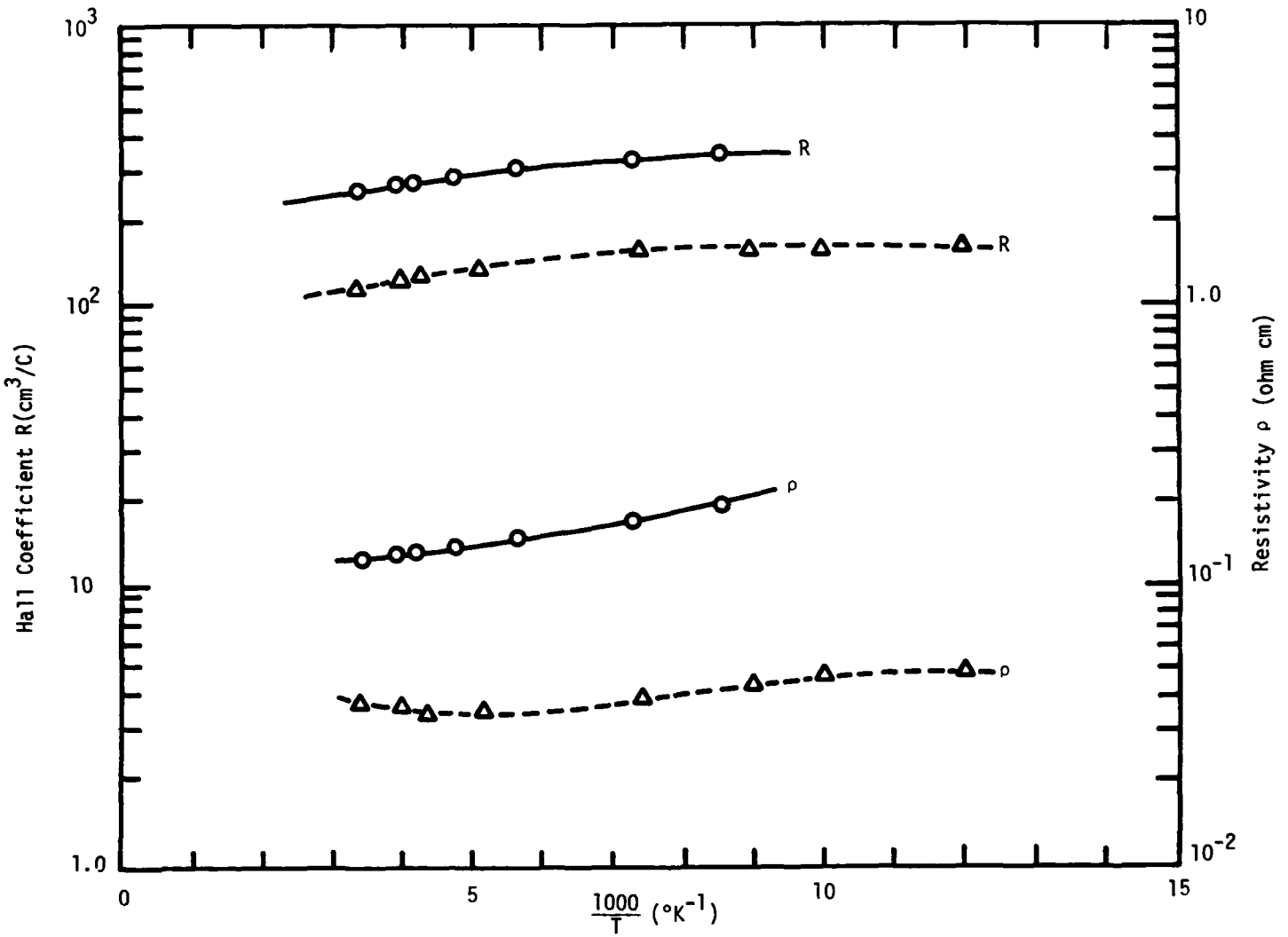


Figure 38. Temperature Dependence of Hall Coefficient (R) and Resistivity (ρ) for Two Unintentionally Doped GaAs Films, MBE 04191 (solid) and MBE 0525II (dotted). Both n-Type Layers were Grown on Cr-doped Substrates.

as mass transfer or the establishment of thermal equilibrium conditions between the doping species and the heated surface of the growing layer. The latter observations are based upon the absence of a pronounced, systematic variation of the doping level as a function of growth rate or substrate temperature. Substituting another dielectric for BeO changed the carrier type and lowered the background concentration. The BeO powder used in fabricating the Thermalox 995 heaters typically contains sulfur at a level of 0.08 percent. The residual sulfur after forming at 1550 °C is believed to be present in the form of compounds. Since sulfur is an n-type dopant with an activation energy of 0.006 eV in GaAs[94], it does match the properties measured for the MBE layers. The porosity of BeO may cause potential contaminants to be trapped in the heater during chemical cleaning operations which remove the polycrystalline GaAs formed on the exposed BeO during a growth run.

4.2.2 Anomalous Low Level Dopant

An anomalous n-type dopant has been observed for layers using the fused quartz radiant heaters described in Section 2.2. Four runs were completed with nominal deposition rates of one micron hr^{-1} and substrate temperatures of 600 °C. Doping profiles for three of the four layers are presented in Figure 39. At the interface between the epi-layer and the substrate the doping level drops sharply from the low $10^{15} cm^{-3}$ level to well below $10^{13} cm^{-3}$ typically observed for Cr-doped GaAs substrates. Corrected Hall mobilities at room temperature were 2363, 5688, and 5250 $cm^2 volt^{-1} sec^{-1}$ for layers A0928TFM, A0930TFM, and A1006TFM, respectively. The plot of Hall mobility versus temperature for layer A0930TFM given in Figure 24 (p. 56) showed signs of saturating at 19,000 $cm^2 volt^{-1} sec^{-1}$ for a temperature of 77 °K.

Layer A1004TFM, the third layer grown in the series, was a high resistivity sample and neither Hall nor Schottky diode measurements could be reliably

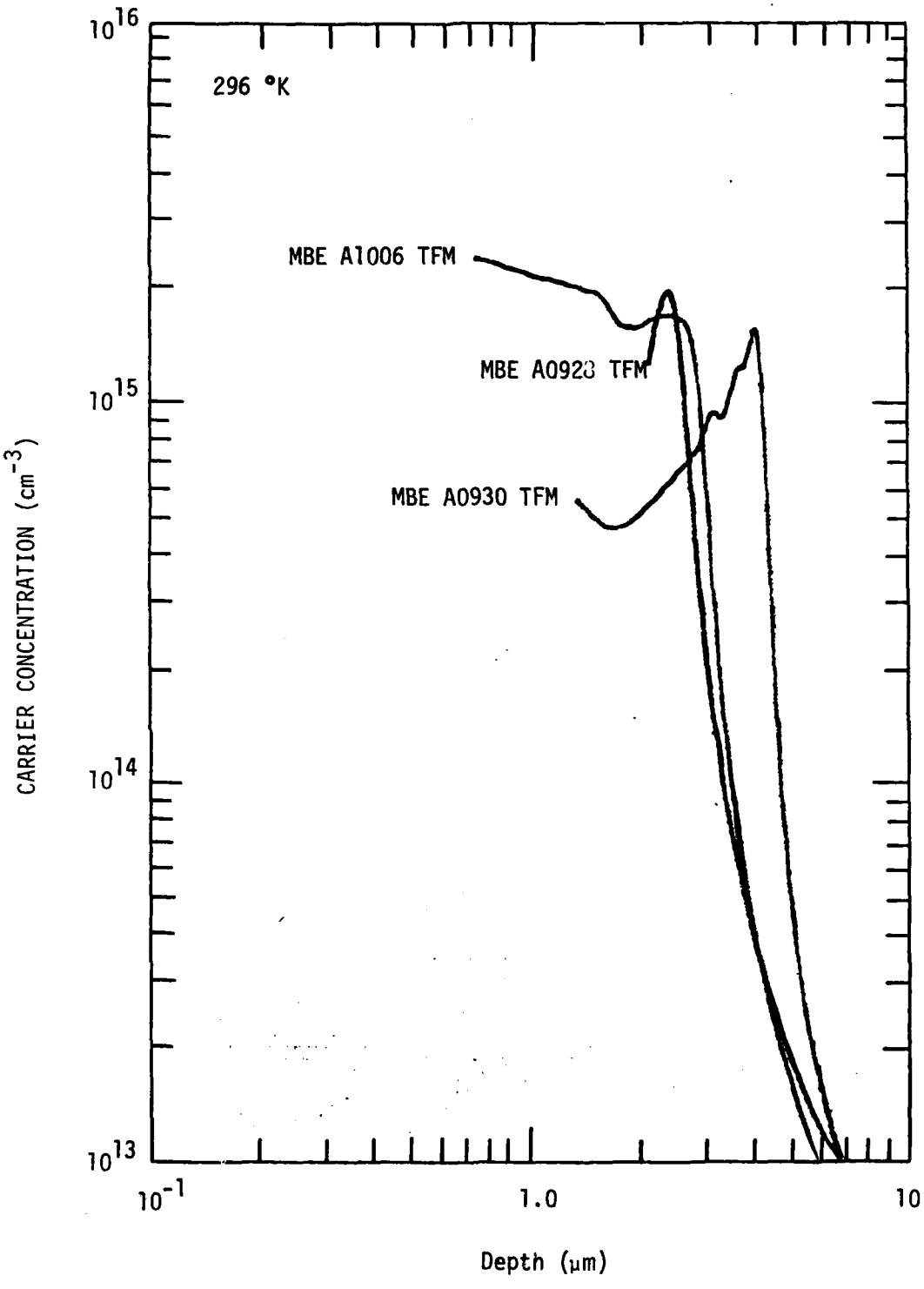


Figure 39. Doping Concentration Profiles for Three MBE Layers Grown on Cr-doped GaAs Substrates. In Each Layer the Unintentional Dopant was n-type.

reproduced. The unintentional background dopant for MBE layers is generally found to be p-type in the low 10^{14} cm^{-3} range. The high resistivity for this layer likely arises from a close degree of compensation.

The electron probe X-ray microanalyzer and an arc emission spectrograph were used to identify potential dopants arising from the 6N indium interface between the GaAs substrate and the Mo carrier plates utilized in growing the first three layers. Traces of zinc and oxygen and possibly tin were found as foreign elements. Tin, if present, was at or below the detection limit of the equipment. No appreciable compensation effects are expected from Zn since it desorbs rapidly from GaAs surfaces[57] held above 175 °C. The Hall data indicate that the dopant is shallow with an activation energy $\leq$ 0.005 eV. Oxygen enters GaAs as a deep donor with an activation energy near 0.75 eV. Tin, on the other hand, is a very shallow donor in GaAs and it has a sticking coefficient of unity. A problem in tagging tin as the background dopant arises since the fourth layer, A1006TFM, which used Ga for the interface metal also shows n-type behavior. Tin was absent in a spectrographic analysis of the 6N Ga. It is doubtful that the Ga oven for this run was already contaminated with tin as the vapor pressure of Sn is 2.0 Torr at the oven operating temperature of 1026 °C. This is inconsistent with the striking uniformity in the doping profile for A1006TFM given in Figure 39. Each layer in the series was grown following a six hour bakeout of the chamber at 100 to 150 °C. Background pressures before deposition fell in the mid 10^{-10} Torr range.

A second run series was initiated following an extended high-temperature outgassing of all ovens, and the installation of the interlock and large As oven. The n-type dopant at a level of approximately 10^{15} cm^{-3} was still

present in the system after five runs. The sixth run in this series MBE A1216 had a relatively uniform doping profile of 1.5×10^{15} cm^{-3}. The layer was grown at a rate of 0.9 $\mu m\ hr^{-1}$ at a substrate temperature of 600 °C. The doping concentration taken from Schottky diode measurements was in fairly good agreement with the Hall concentration of 2.6×10^{15} cm^{-3}. Mobilities were 6848 and 20860 $cm^2\ V^{-1}\ sec^{-1}$ at 296 and 77 °K, respectively. These hall data include the correction for the finite size contact pads at the corners of the square van der Pauw sample[64].

Eleven out of 13 runs on the large fused quartz radiant heaters yielded layers doped n-type at levels of low 10^{15} cm^{-3}. The evidence indicates that this unintentional dopant is silicon entering a Ga-site. An elemental analysis of the Ga taken from the Ga oven following these two separate run series showed Si at the levels of 10-20 ppm and 40 ppm. No Si was detected in the initial oven loads. Hot Ga reduces refractory oxides and SiO could be released from the top surface of the fused quartz heater. However, judging from the discoloration in the Ta film after several hours of operation, another potential source of the unintentional doping is a Ta-SiO_2 reaction. Black body calculations using the electrical power input to the Ta film suggest that the Ta film on the large fused quartz heater was operating approximately 100 °C higher than the small fused quartz heaters (Section 4.3.2). The absence of Si on acceptor sites in the photoluminescence spectra at 1.485 eV for layer MBE A1216 (Figure 35, p. 79) is consistent with growth under As-stabilized conditions. When the large fused quartz heaters were replaced with the Mo block, radiant Ta coil heater (Figure 9, p. 29), the undoped layers contained a dominant acceptor at

approximately 2 x 10^{14} cm^{-3}.

4.3 UNINTENTIONAL p-TYPE DOPANTS

4.3.1 Hot Stainless Steel

A primary source of unintentional doping contamination arises from hot stainless steel elements illuminated by the molecular beam from the Ga oven. This source is a dynamic function of system components and operation. A build-up of alloyed material was observed on the stainless steel shutter and the tip of the stainless rod supporting the Ga oven. Examination of the shutter after approximately 70 runs showed that the reaction had become so extensive that tiny pin holes punctured the section immediately in front of the Ga oven.

Table 5 tabulates the basic deposition parameters, dopant properties, and system parameters for the p-type layers grown before the stainless shutters, bearing mechanisms and deposition shields were replaced by Ta elements. As discussed previously, growth on BeO heaters predominately yields n-type material. Doping from hot stainless was only dominant in the presence of a sufficient quantity of the acceptor to over-ride the donor contributed by the BeO heater. It is reasonable that a slightly lower acceptor background was observed with the small fused quartz heaters since the Ga oven was thermally outgassed before runs 0603I and 0620I, the Ga shutter was frequently cleaned, the the cold trap assembly supporting the ovens was operational.

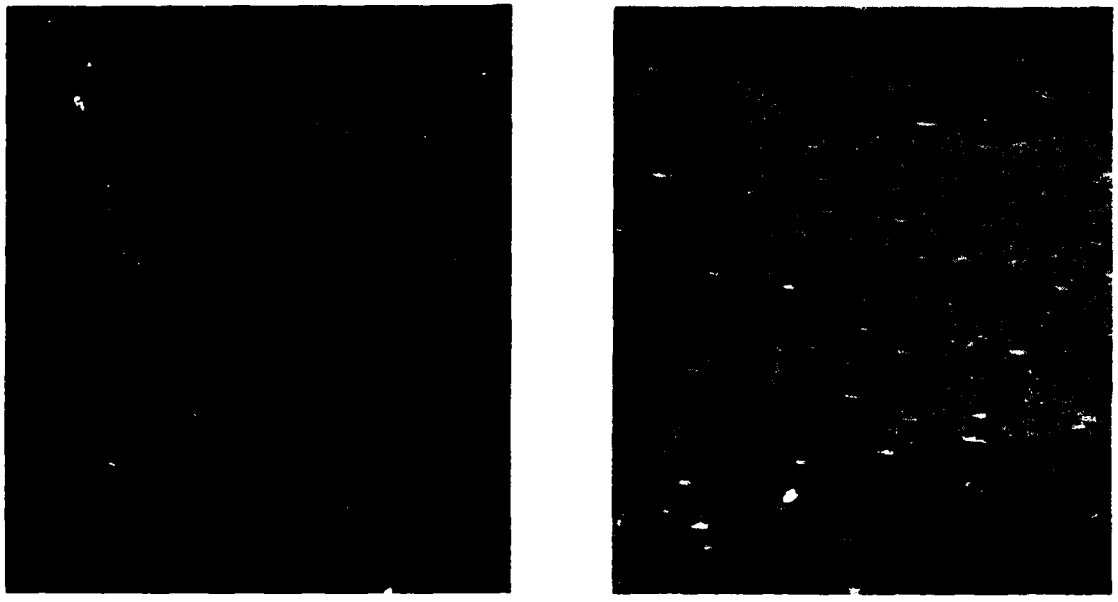
A photomicrograph of the surface of MBE 0407III is displayed in Figure 40a. The ridge structure for this specimen is duplicated on layers 0105III and 0460I. There is a reduced incidence of the ridges for the thick layer MBE 1207III shown in Figure 40b. A rippled surface structure has been reported

Table 5. Summary of Deposition Parameters, Dopant Properties, and System Parameters During Background Doping Studies of p-type GaAs Grown by MBE on Cr-Doped Substrates.

	DEPOSITION PARAMETERS			DOPING PROPERTIES(296°K)			SYSTEM PARAMETERS		
MBE Layer	Thickness (μm)	Growth Rate (μm/hr)	$T_{substrate}$ (C°)	Carrier Type	Mobility ($cm^2V^{-1}sec^{-1}$)	Concentration (cm^{-3})	As Source Purity	Cold Trap Operating	Substrate Heater Type
1207III	5.6	0.7	550	p	214	1.2×10^{17}	5N	no	BeO
0105III	1.5	0.4	550	p	256	2.1×10^{17}	5N	no	BeO
0406I	3.0	1.0	560	p	118	7.3×10^{16}	5N	no	BeO
0407II	2.5	1.0	540	p	82	1.4×10^{17}	5N	no	BeO
——→									
0603I	1.7	0.4	620	p	371	1.1×10^{15}	6N	no	FQ
0607III	1.6	0.4	640	p	285	1.0×10^{16}	6N	no	FQ
——→									
0620I	1.4	0.7	580	p	269	4.5×10^{16}	6N	yes	FQ
0624II	1.2	0.6	600	p	263	7.0×10^{15}	6N	yes	FQ
0708I	1.6	0.8	600	p	235	6.8×10^{16}	6N	yes	FQ
0712I	1.7	0.9	575	p	244	9.7×10^{15}	6N	yes	FQ
0713II	1.7	0.8	575	p	228	5.4×10^{15}	6N	yes	FQ

Concentrations for the above samples taken from Hall measurements

——→ Ga oven outgassed and reloaded



500x (a)

500x (b)

Figure 40. Interference Contrast Micrographs of the Ridge Structure Observed on the Surface of MBE0407II (a) and MBE1207III (b). The GaAs Epi-Layers were Grown on the (001) Surface of Cr-doped GaAs Substrates.

for Mn-doped GaAs layers (1 x $10^{17}cm^{-3}$) which is attributed to surface segregation of the dopant during MBE growth[23]. Similar segregation effects may be operating in the present data.

The results of Hall measurements are plotted in Figure 41 for two representative layers. The strong dependence of R upon inverse temperature indicates that the acceptor dopant has a relatively large activation energy. Detailed fitting of the Hall data for layers 1207III, 0105III, 0708I, 0712II, and 0713II yields activation energies of 0.124, 0.180, 0.050, 0.094, and 0.290 eV, respectively. The incorporation of Be from the BeO substrate heater can largely be eliminated as an acceptor dopant since Be doping does not introduce changes in the surface morphology of GaAs epi-layers[23] and the binding energy for Be in GaAs has been established as 0.028 eV[80].

Following the 0700 run series, specimens of the Ga oven load, the stainless steel shutter, and flakes from the shutter surface were examined using arc spectroscopy and the electron microprobe. The analytical results are given in Table 6. The table shows that the Ga oven load was contaminated with elements contained in the stainless steel shutter. Since the shutter was thinly coated in some areas, stainless steel elements are expected in the last column. The intensity of elements marked by *trace?* either fell at the limits of detection or were indistinguishable from elements in the carbon electrode. Detection sensitivities ranged from one part in 10^6 to one part in 10^9. A fresh sample of 6N Ga analyzed with arc spectroscopy confirmed the specified purity of the initial Ga supplied by Alusuisse. The elements Mn, Fe, and Ni enter GaAs as relatively deep acceptors with activation energies $\geq$ 0.096 eV. Copper is a multi-level acceptor in GaAs (0.025, 0.15, 0.24, and 0.51 eV) and is present in the system in the flange gaskets and

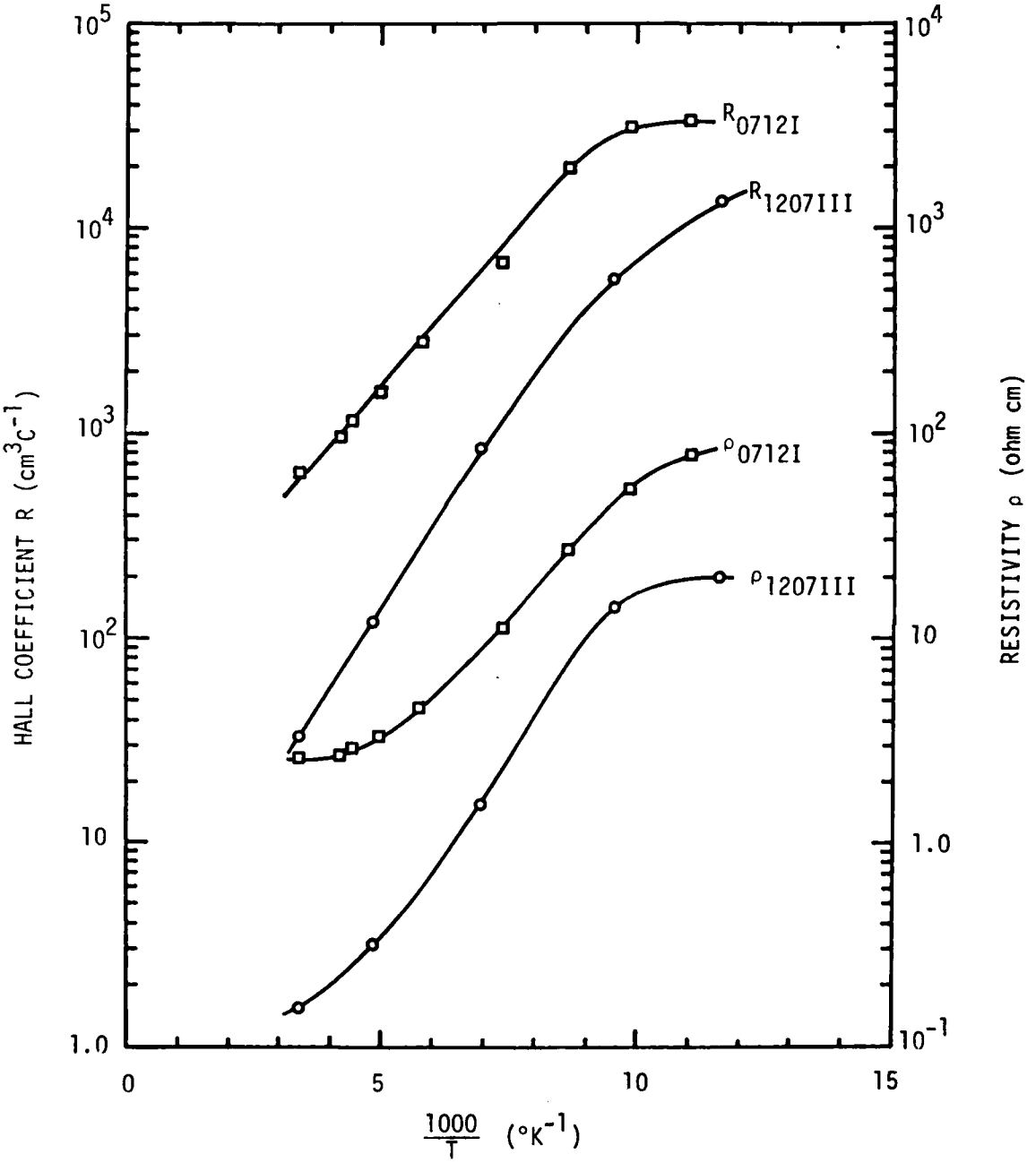


Figure 41. Temperature Dependence of Hall Coefficient and Resistivity for Two Unintentionally Doped p-type GaAs Layers Grown by MBE.

Table 6. Arc Spectroscopy and Electron Microprobe Analyses of the Shutter (Stainless) and Load (6N Ga) for the Ga Oven After 14 Hours of Operation.

Element	6N Ga (Fresh)	Oven Load Ga	Flakes Peeled from Shutter	Shutter
Arsenic	**	med. strong	strong	strong
Chromium	**	**	trace ?	trace to strong
Copper	**	trace	**	**
Gallium	very strong	strong	strong	strong
Iron	**	trace ?	trace	trace to strong
Magnesium	trace ?	**	**	**
Manganese	**	trace ?	trace	trace to med. strong
Nickel	**	trace	trace	trace to strong
Oxygen		trace	**	trace
Silicon	**	**	trace ?	trace to med.

electrical feedthroughs. Some runs employed small compression pads of copper beneath thermocouple and electrical leads clamped to the substrate heater.

Additional evidence that hot stainless steel is ultimately a potential dopant source for GaAs layers grown by MBE was demonstrated by the reversion from p-type to compensated n-type growth on BeO heaters when the Ga oven was outgassed and a new stainless shutter was installed. Completely removing hot stainless steel from the reaction region effectively eliminated the high acceptor doping and the basic background concentration was either p-type below 9×10^{15} cm^{-3} (Section 4.3.2) or the anomalous donor (Section 4.2.2) doping at approximately 1×10^{15} cm^{-3}.

4.3.2 Residual Background

The residual background for unintentionally doped GaAs grown by MBE is typically dominated by a compensated acceptor level. General deposition conditions and electrical properties for representative layers are given in Table 7. All substrates in the 0800 series except 0817II were heated with the small fused quartz/Ta film heaters. A boron nitride/Ta film heater was employed for 0817II. This heater received only limited testing since it required high input powers (80 W vs. 20-30 W for the small fused quartz heaters), and there was no significant improvement in the background doping level. The low mobilities observed for 0811I and 0822II are believed to be associated with crystalline lattice imperfections. Evidence of a faint polycrystalline ring structure underlying the primary spot pattern was discernable in electron diffraction analyses of layer 0815I. Ten p-type layers grown with the small fused quartz heater had carrier concentrations lying between 2×10^{14} and 8×10^{15} cm^{-3}, room temperature mobilities ranging between 180 and 370 cm^2 V^{-1} sec^{-1}, and activation energies between

Table 7. Deposition Parameters and Electrical Properties (296°K) of n-type GaAs Layers Grown by MBE on Cr-Doped Substrates

MBE Layer	Thickness (μm)	Growth Rate (μm/hr)	$T_{substrate}$ (°C)	Carrier Type	Concentration (cm^{-3})	Mobility ($cm^2V^{-1}sec^{-1}$)
0811I	3.3	0.5	585	p	$4.6\ 10^{14}$	188
0815I	4.1	0.7	590	p	$2.1\ 10^{14}$	*
0817II	1.2	0.4	585	p	$8\ 10^{15}$	*
0822III	2.5	0.4	590	p	$1.7\ 10^{15}$	182
0829III	7.1	1.4	580	p	$6.9\ 10^{15}$	277
A0327	6.0	1.5	600	p	$1.9\ 10^{14}$	334

* Schottky barrier diode used for electrical measurements.

0.05 and 0.30 eV. The second type of growth encountered with this heater exhibited the high resistivity expected for closely compensated material. Six layers were grown which fell into this category. For example, two layers less than one micron thick, 0809III and 0810I, had probe to probe breakdown voltages greater than 160 volts. The I-V characteristics using evaporated Au(80%)/In(20%) contacts, Ag(82%)/In(12%)/Mg(6%) contacts, or 20 mil diameter In spheres containing one percent Zn^{95} also indicated high resistivity material.

Layer A0327 represents the residual acceptor at low 10^{14} cm^{-3} level observed for specimens mounted on a Mo block radiantly heated by a Ta filament. Other important system characteristics included the interlock and the extensive use of Ta for heated structural elements in the growth region. Fitting the Hall data to a single acceptor model yielded an activation energy of 0.027 $\pm$ 0.003 eV. It is interesting to note that this is close to the binding energy reported for carbon (0.026 eV)[80]. The RGA spectrum does indicate that traces of water vapor, CO, and CO_2 are present during MBE growth. The mobility measured at liquid nitrogen temperatures for MBE A0327 was 4578 cm^2 V^{-1} sec^{-1}.

4.4 SURVEY OF LABORATORIES USING MBE TO GROW GaAs

A survey by laboratory of GaAs grown by MBE is given in Table 8. The goal of this survey was to assess the state-of-the-art of unintentionally doped material as of August - December 1977. The survey showed that MBE layers tended to have a dominant acceptor concentration of 10^{14} - 10^{15} cm^{-3} and room temperature mobilities approaching the theoretical limit[62] for lattice scattering of 400 cm^2 V^{-1} sec^{-1}. Additional features of the entries in table 8 are highlighted below.

Table 8. Survey by Laboratory of Deposition Parameters and Electrical Properties of Unintentionally Doped GaAs Layers Grown by MBE - 1977

Laboratory	Thickness (μm)	Growth Rate (μm hr^{-1})	T_{sub} (°C)	Carrier Type	Concentration (cm^{-3})	Mobility (297°C) ($cm^2V^{-1}sec^{-1}$)	Activation Energy (eV)	Likely Dopant	Reference
Air Force Avionics Lab. Wright-Patterson AFB, Ohio	1.0-10.0	~ 0.2	580	p	10^{13}	100	*	*	C. Litton[96]
Bell Laboratories Murray Hill, N.J.	5.0	1.0	600	p	3.7×10^{14}	332	*	C	A.Y. Cho and J.R. Arthur[57]
Georgia Tech Atlanta, Ga.	1.2-14.2	0.3-3.0	575-620	p	$2x10^{14}$-$8x10^{15}$	180-370	0.05 - 0.30	Cu,Mn	
Lincoln Labs, MIT Cambridge, Mass.	2.0	~1.0	575	p	10^{13} - 10^{14}	~300	*	unknown, C?	A.R. Calawa[96]
Phillips UK Redhill, England	5.0	1.0	520	p	3×10^{14}	~400	0.023	C, defect	C.T. Foxon[96]
Rockwell Science Cen. Thousand Oaks, Calif.	2.0	5.0-7.0	530-580	n or p	10^{14}-10^{15}?	*	*	*	L. Szalkowski[96]
IBM Research Center Yorktown Heights, N.Y.	5.0	0.3-1.0	580	p	10^{15}-10^{16}	300-400	shallow	C	L.L.Chang[96]
Thomson-CSF Orsay, France	1.0-2.0	0.5	530	p	$5x10^{14}$-$8x10^{15}$	300-430	*	*	N.T. Linh[96]
Tokyo Inst. of Tech. Tokyo, Japan	0.5-2.0	0.5-2.0	550-600	p	~10^{14}	*	*	C,Mn(?)	K. Takahashi[96]
Varian Vacuum Div. Palo Alto, Calif.	2.0	1.0	~600	p	3×10^{15}	120	0.14	Cu, Ga vacancy	P. Luscher[96]

The doping concentrations entered in Table 8 are the quantity N_A-N_D. The background doping of layers formed at Bell Laboratories typically occurs at 2×10^{14} cm^{-3}. The data shown in the table were selected because of the availability of corresponding mobility information. A more sensitive indication of the crystalline quality of this layer is the 77 °K mobility of 5210 cm^2 V^{-1} sec^{-1}. This compares favorably with lattice limited mobilities of 9000 cm^2 V^{-1} sec^{-1} reported for high purity p-type GaAs[62]. Although the doping levels for the Georgia Tech layers were relatively low, subsequent analysis revealed several potential sources of the acceptor doping related to system construction and operation during this period. Electrical measurements as a function of temperature were not available for the material grown by AFAL, Lincoln Laboratories, Thomson-CSF, or Tokyo Institute of Technology. Difficulties in obtaining ohmic contacts limited Rockwell's electrical characterization of their unintentionally doped material. P. Luscher emphasized the preliminaty nature of the Varian results. In general, high resistivity layers 10^2 to 10^3 ohm cm were obtained for unintentionally doped GaAs grown by the Tokyo Institute of Technology and detailed electrical measurements could not be completed for these layers.

Many laboratories (AFAL, Bell, Georgia Tech, etc.) have subsequently grown unintentionally doped layers with improved electrical properties since the compilation of Table 8. For example, in our present system configuration the dominant acceptor appears to be fairly shallow (0.027 eV) with a doping concentration in the low 10^{14} cm^{-3} range. No fundamentally new features have been reported, however, that significantly alter the results presented in Table 8.

5.0 INCORPORATION OF INTENTIONAL DOPANTS

5.1 INTRODUCTION

Many of the group II and group VI elements traditionally employed for doping LPE and CVD GaAs layers have such high vapor pressures and low sticking coefficients that they cannot be easily employed in MBE GaAs. The most useful shallow n-type dopants for MBE layers are the amphoteric group IV elements Sn, Ge, and Si[12,15-19]. These elements are readily incorporated as donors on Ga sites during MBE growth under As-stabilized conditions. Far infrared spectroscopic techniques fix the ionization energies of Ge and Si at 0.005949 and 0.005759 eV, respectively[97]. Each of these dopants has potential drawbacks. Tin exhibits surface segregation effects[18,29,30,98,99], Ge-doped layers are easily compensated[15,100], and Si-doped layers are subject to unintentional doping by impurities released from the doping oven due to the high temperatures required to obtain practical doping levels in device structures.

A number of elements including Ge, Mn, Mg, Be, and Zn have been employed as p-type dopants for GaAs grown by MBE[12,15,16,19-23]. Not all of these elements are equally useful, however. Germanium requires careful control of the As/Ga ratio, Zn and Mg have low sticking coefficients, and Mn enters as a deep acceptor (0.113 eV)[20]. Beryllium is readily incorporated into MBE GaAs as a shallow acceptor with a sticking coefficient near unity. Additional characteristics of intentionally doped, n- and p-type GaAs layers are highlighted in the following sections.

5.2 GENERAL DEPOSITION CHARACTERISTICS

A useful theoretical relationship between the dopant oven temperature and the doping concentration can be derived from expressions describing the

molecular flux effusing from a Knudsen cell. Following the analysis given in Section 2.1 (pp. 11) the dopant flux F_d (molecules cm^{-2} sec^{-1}) arriving at the substrate is expressed as

$$F_d = 3.514\ 10^{22}\ s^2\ (h^2 + s^2)^{-1}\ p^*\ (MT)^{-1/2} \qquad (18)$$

where s = radius of oven aperture (cm),

h = oven to substrate spacing (cm),

p^* = equilibrium vapor pressure (Torr),

M = molecular weight, and

T = temperature (°K).

The configuration parameters for the MBE system at Georgia Tech presently employ s = 0.377 cm and h = 6.0 cm. Assuming a growth rate of 1.0 μm hr^{-1} and a sticking coefficient of unity, then the doping concentration can be computed as a function of the oven temperature since $p^*(T)$ is available in vapor pressure tables[56]. Figure 42 provides a convenient summary of the theoretical calculations for ovens loaded with Mn, Sn, Be, Ge, and Si.

5.3 PROPERTIES OF DOPED MBE GaAs

The intentionally doped GaAs layers have been grown under As-stabilized conditions with a substrate temperature of 560 - 600 °C and a nominal growth rate of 1.0 μm hr^{-1}. Tin (5N) and Ge (metal 6N) were used for the n-oven loads and Be (3N5) was used for the p-oven loads. Most of the n- and n^+-layers were grown on (001) n^+-substrates. Doping concentrations for these layers were measured by C-V profile techniques. Step etching in conjunction with staircase profiles of doping oven temperature yielded multiple $N(T_{oven})$ calibration points with a minimum number of growth runs. Carrier concentrations were also measured by Hall techniques for layers grown on Cr-doped

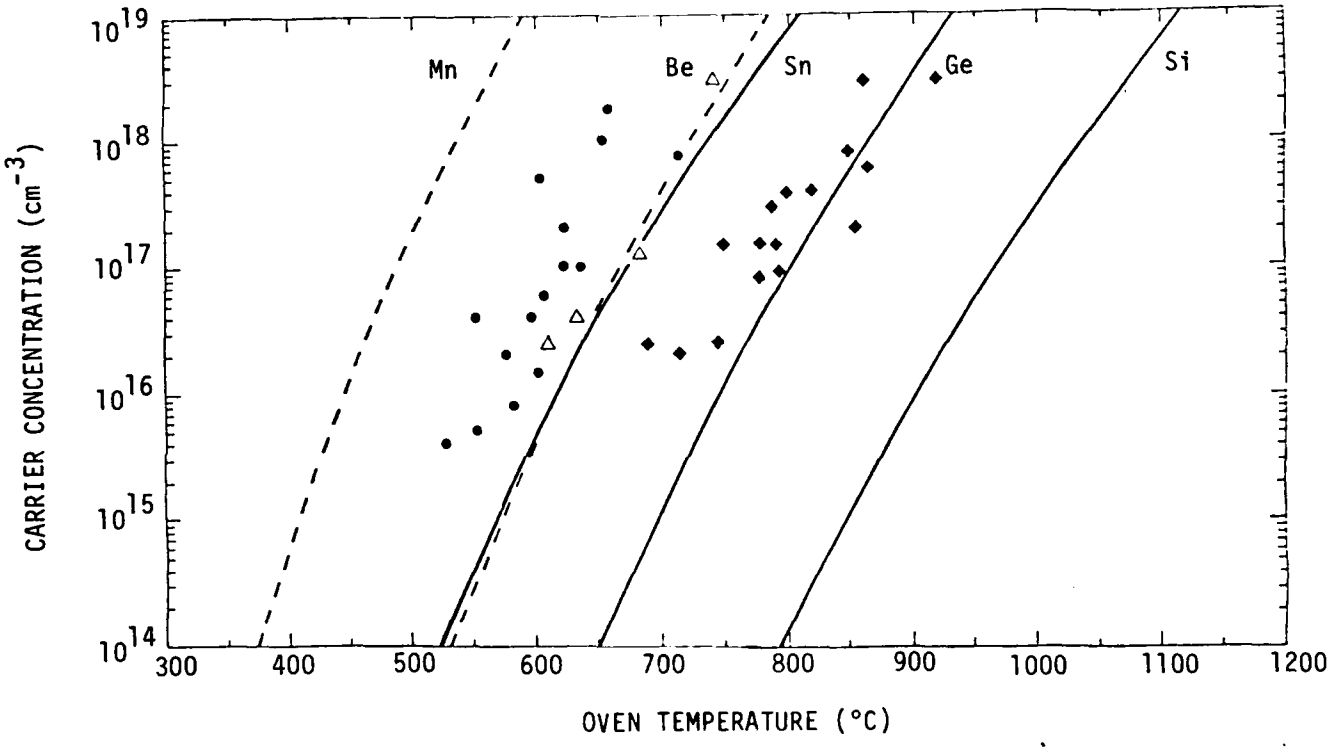


Figure 42. Doping Concentration vs. Oven Temperature for GaAs Grown by MBE Under As-Stabilized Conditions. Solid Curves: n-Type; Dashed Curves; p-Type. Theoretical Curves Based Upon Growth Rate = 1.0 μm hr^{-1}, Source-to-Substrate Spacing of 6.0 cm and Oven Diameters of 0.75 cm. Actual concentrations Determined by Hall and C-V Profile Measurements are Plotted for Sn (●), Ge (◆), and Be (△) Doped Layers.

substrates.

Experimentally measured carrier concentrations and oven temperatures are compared with the theoretical values in Figure 42. The general agreement between the theoretical relationship and the measured carrier concentrations as shown in Figure 42 provides a strong indication that the sticking coefficients for Sn, Be, and Ge are approximately equal to unity for the given growth conditions. The displacements between the experimental and theoretical data are attributed to small temperature offsets between the loads and the monitoring thermocouples inserted in the rear of the doping ovens. The scatter arises principally from slight run-to-run changes in the growth rate and the geometric factors associated with the angular relationships between the Ga and the doping ovens.

Table 9 summarizes the deposition parameters and electrical properties at room temperature for doped GaAs layers grown in semi-insulating substrates. The relationship between mobility and carrier concentration is graphically displayed in Figure 43. The solid curve drawn on the figure passes through experimental data reported for N-type GaAs layers grown by MBE[16,22] and LPE[101]. For concentrations greater than approximately 10^{17} cm^{-3}, the solid curve lies slightly below the theoretical drift mobility versus free electron concentration variation for ideal extrinsic n-type GaAs (300 °K) where compensation is negligible[63]. The dashed curve in Figure 43 is a theoretical curve for p-type GaAs based upon a Brooks-Herring formulation[62]. Since the latter curve follows the general trend of other experimental data for p-GaAs, the electrical characteristics of the Be-doped layers look quite encouraging. The Sn- and Ge-doped layers also exhibit the high carrier mobilities needed for good device performance.

Table 9. Deposition Parameters and Electrical Properties (296 °K) Doped GaAs Grown by MBE on Cr-Doped Substrates

MBE Layer	Thickness (μm)	Growth rate ($\mu m\ hr^{-1}$)	$T_{substrate}$ (C°)	Dopant	Carrier Type	Concentration (cm^{-3})	Mobility ($cm^2V^{-1}sec^{-1}$)
A1228	1.8	0.9	600	Sn	n	3.9×10^{15}	5814
A0222	3.8	1.4	600	Sn	n	6.0×10^{15}	6800
A0227	5.0	2.0	600	Sn	n	8.0×10^{15}	5768
A1222	1.9	0.9	600	Sn	n	6.9×10^{16}	4321
A1221	1.6	0.8	600	Sn	n	6.0×10^{17}	5068
A1220	1.4	0.9	600	Sn	n	1.81×10^{18}	2690
A0302	1.0	0.4	600	Sn	n	3.3×10^{18}	2510
A0707	3.7	0.9	560	Ge	n	3.6×10^{16}	5236
A0628	5.6	1.4	560	Ge	n	4.0×10^{16}	4084
A0629	6.3	1.6	557	Ge	n	8.0×10^{16}	4765
A0811	2.8	0.9	560	Be	p	2.5×10^{16}	370
A0808	4.1	1.4	555	Be	p	4.0×10^{16}	306
A0804	4.4	1.5	557	Be	p	1.0×10^{17}	309
A0810	3.3	1.1	560	Be	p	2.6×10^{18}	153

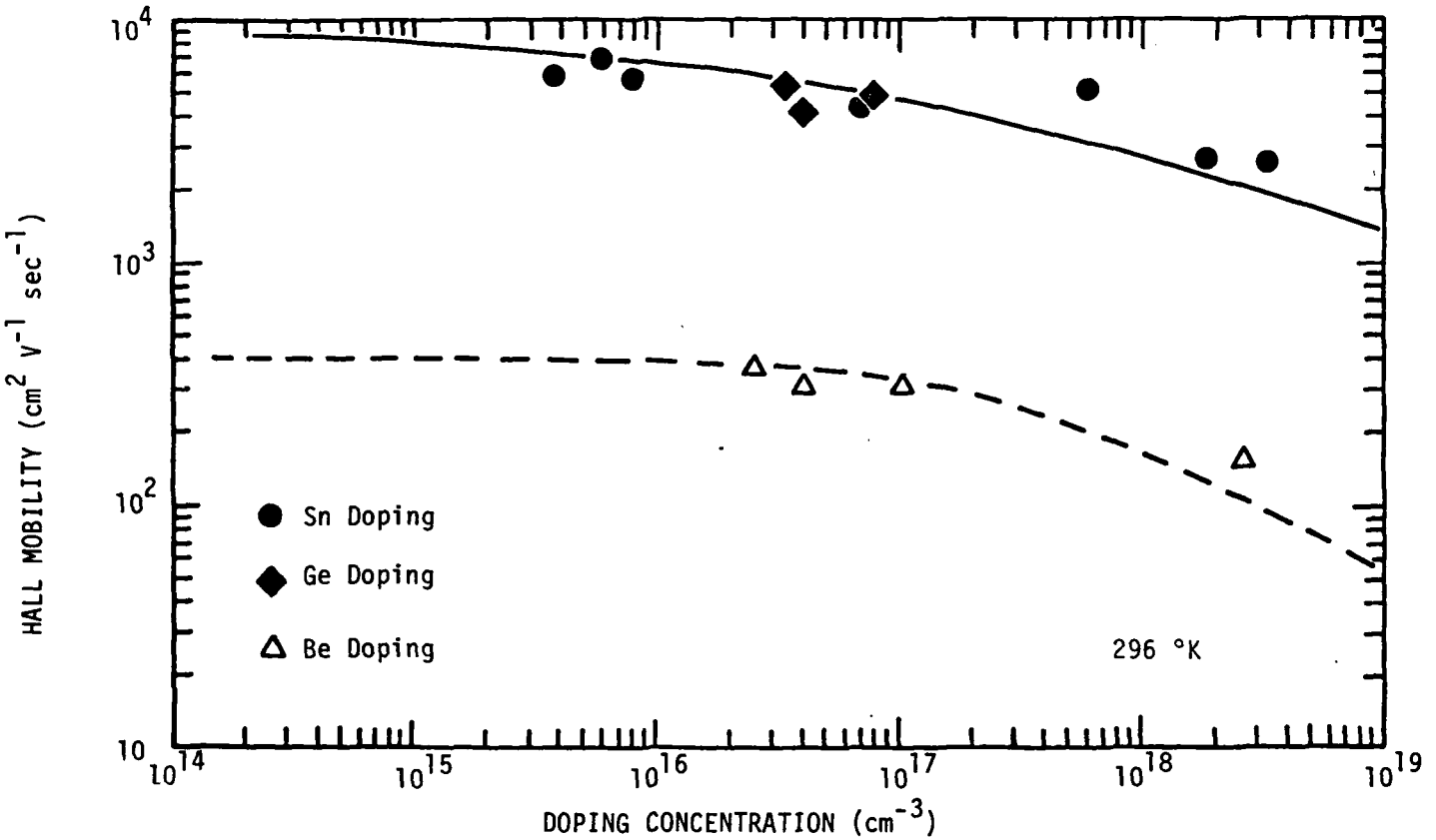


Figure 43. Hall Mobilities vs. Doping Concentration for MBE GaAs Layers Grown under As-Stabilized Conditions. Solid Curve: Typical Published Data for n-GaAs Grown by MBE and LPE[16,22,101]. Dashed curve: Theoretical Data for p-GaAs[62].

5.3.1 Sn-Doped, n-Type Layers

The doping of GaAs epilayers was initiated using tin as the doping species. The tin oven temperature was maintained at a constant value throughout the growth of a given step or layer. Other deposition conditions included a substrate temperature of 600 °C and an As/Ga ratio of approximately 100. In contrast to the results of Joyce and Foxon[19], the Hall data show that these growth conditions yield little increase in auto-compensation for Sn-doping levels exceeding 5×10^{17} cm^{-3}.

The uniformity of tin incorporation has been examined in detail using C-V measurements of Au Schottky diodes. A Materials Development Corporation automatic doping profiler provided profiles directly from the C-V data. While the profiler responds accurately to capacitive components across the test terminals, false profiles can be returned when the diode Q drops below 100. Therefore, doping profiles were also computed point by point with the aid of a Boonton 75D capacitance meter which monitored both the real and reactive components of diode impedance. The mathematics underlying this approach is given in Appendix I. Doping concentrations determined by both techniques are compared for two Sn-doped layers in Figure 44. It is clear that segregation cannot be accurately estimated by the automatic doping profiler.

In order to quantify the segregation, the data were fitted to a power curve of the form

$$N(x) = \alpha x^{\beta} \qquad (19)$$

where x is the depth into the semiconductor layer. For the point by point results given in Figure 44, $\beta = -0.16$ and -0.33 are obtained for MBE A1221

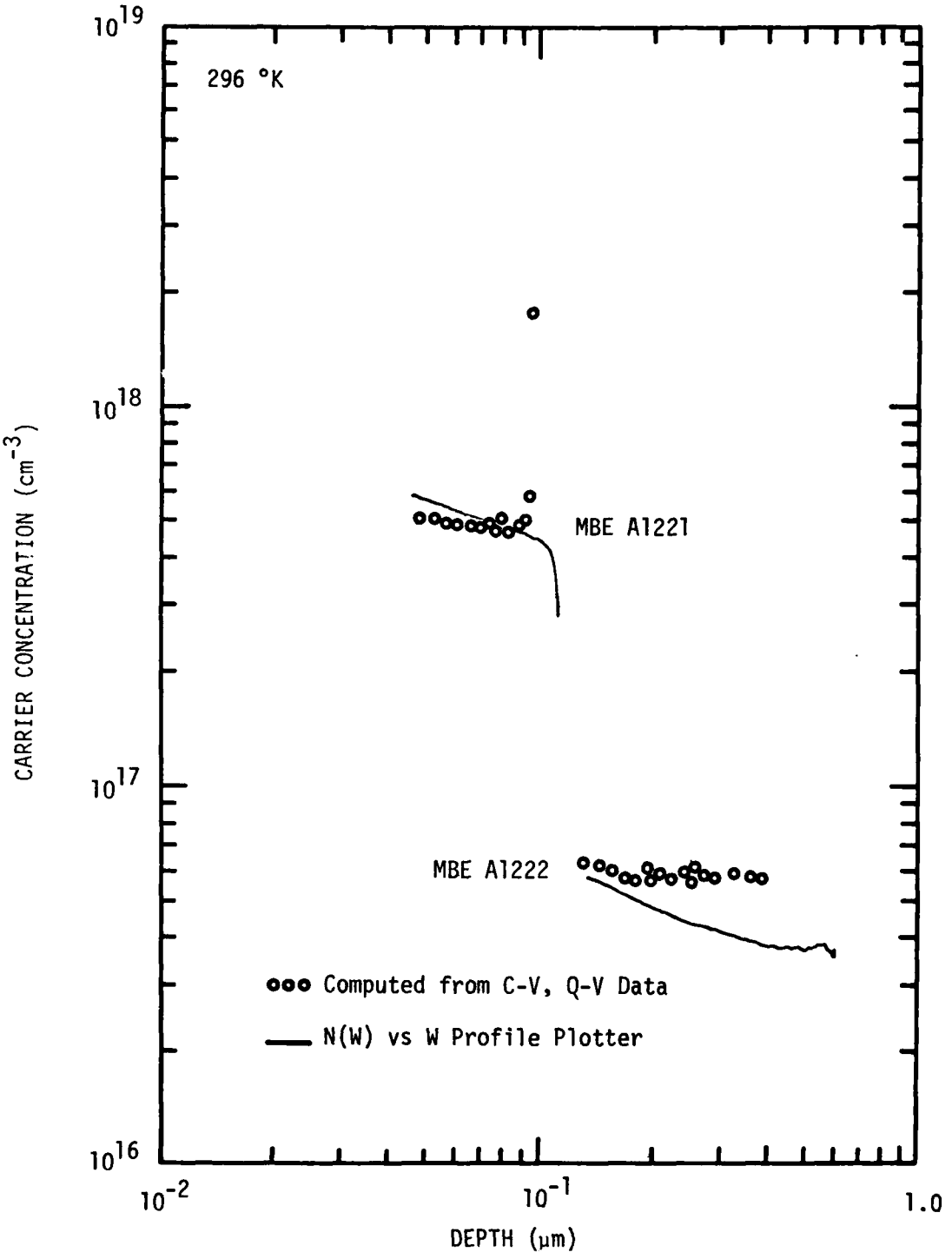


Figure 44. Doping Concentration Profiles for Sn-Doped Layers of GaAs Grown at a Substrate Temperature of 600 °C. The Doping Profile Plotter is Compared to Profiles Computed from Point by Point Measurements of C(V) and Q(V) for the Same Schottky Diodes.

and Al222, respectively. With a uniformly doped layer, $\beta = 0$. The segregation shown in Figure 44 is smaller than $\beta = -0.75$ computed for the thin (0.45 μm) Sn-doped layer grown by Wood[30] at a substrate temperature of 597 °C. The MDC profiler plot of MBE Al222 yields $\beta = -0.47$. The concentration of this layer is similar to the Sn-doped layer[29] formed at a substrate temperature of 560 °C. The profiles for the latter layer likewise have a similar power curve variation with $\beta = -0.44$.

We conclude that there is evidence for limited Sn segregation even in relatively thick layers with high As/Ga ratios and $T_{substrate} = 600$ °C. As indicated in Section 7.1, a more serious problem arises at interfaces where doping concentrations change abruptly. These effects have been explained in terms of a surface rate limited mechanism which requires the establishment of a net surface concentration of Sn before significant incorporation occurs in the epi-layer[99]. The unincorporated tin continues to remain at the surface throughout the remainder of the layer growth[98].

5.3.2 Ge-Doped, n-Type Layers

Hall measurements given in Figure 43 for the Ge-doped layers indicate that the room temperature mobilities are similar to the mobilities measured for Sn-doped MBE layers. At 77 °K the lightly doped sample had a mobility of 9317 $cm^2\ V^{-1}\ sec^{-1}$ and a carrier concentration of 2.9×10^{16} cm^{-3}. A total impurity concentration of 5.9×10^{16} cm^{-3} is estimated for this layer[93]. The compensation ($N_A/N_D = 0.35$) potentially arises from Ge occupation of Ga sites. This value is slightly higher than the N_A/N_D ratio = 0.25 based on the intrinsic compensation of Si, Ge, and Sn in GaAs grown by vapor phase epitaxy[102].

5.3.3 Be-Doped, p-Type Layers

An ohmic contact (Ag/In/Mn) and Al Schottky diodes (6.0 mils diameter) were formed on the top surface of layer A0811. Carrier concentrations given by the Hall data in Table 9 and profile measurements using the Schottky diodes agreed within 20 percent. While there was evidence of a slight increase in doping level near the surface, $|\beta_{Be}| \leq 1/2\ |\beta_{Sn}|$.

Figure 45 presents the temperature dependence of the Hall mobilities measured for MBE layers A0808, A0810, and A0811. The dotted line plots an empirical expression [62]

$$\mu = 400\ (300/T)^{2.3} \qquad (20)$$

which represents the lattice scattering contribution to hole mobility in GaAs. As classically illustrated by the figure, significant departures from lattice scattering are observed for the more heavily doped layers as carrier scattering by impurities begins to dominate the transport processes. The mobility versus concentration behavior near 77 °K compares favorably with the optimum data[102] compiled for p-type GaAs grown by other techniques.

Beryllium appears to be entering GaAs grown by MBE as a simple acceptor. Activation energies were estimated by fitting the low temperature data of MBE A0811 and MBE A0808 to a single acceptor model with no compensation[104]. These data yield activation energies of 0.024 and 0.029 eV, respectively. High resolution photoluminescence studies[80] fix the binding energy of Be in GaAs at 0.028 eV.

In view of incorporation and electrical characteristics shown above and the desirable diffusion properties in as-grown layers[105], beryllium is a useful acceptor dopant for MBE GaAs devices. The fabrication and evaluation

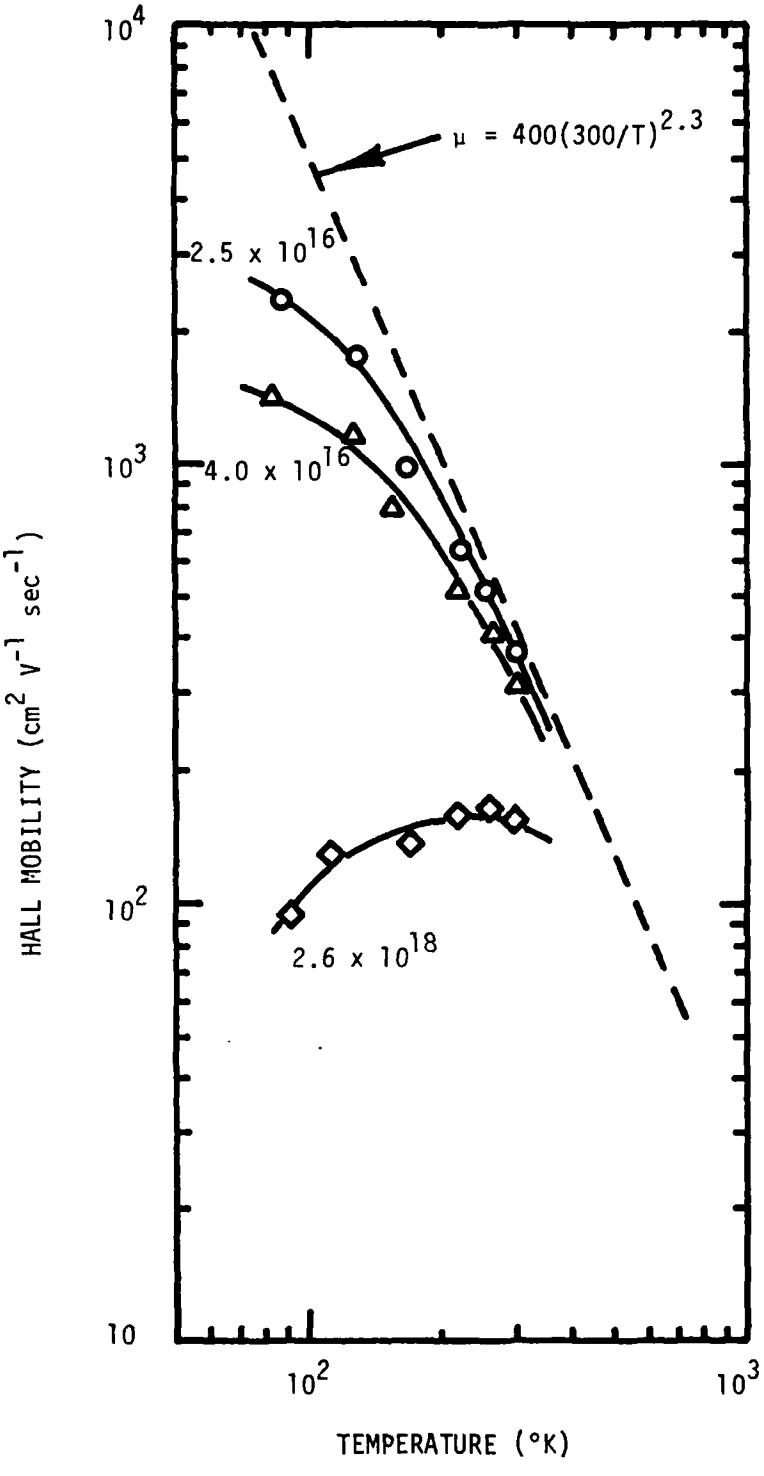


Figure 45. Hall Mobilities for Be-Doped GaAs as a Function of Temperature and Room Temperature Hole Concentration

of p-n junction IMPATTs and varactors using Be and Ge dopants is described in Sections 7.3 and 7.4.

6.0 METAL SEMICONDUCTOR INTERFACE STUDIES

6.1 INTRODUCTION

Fundamental differences are observed in the electrical properties of Au, Ag, and Al Schottky barriers formed on freshly grown and oxidized (001) surfaces of GaAs layers deposited by MBE. A number of microwave devices such as mixer diodes, IMPATTs, and MESFETs utilize Schottky barriers on n-type GaAs. The performance of these devices is controlled by such parameters as barrier height, breakdown voltage, and series resistance. While the nature of Schottky barriers deposited on cleaved semiconductor surfaces has been investigated by several laboratories[106,107], most of the investigations of Schottky barriers formed on GaAs layers configured for device packaging incorporate a thin oxide interface between the metal and semiconductor surfaces[108-110]. The UHV environment of the MBE system is particularly convenient for conducting a study of Schottky barrier characteristics on freshly grown planar layers of GaAs. In the following investigation a unique experimental configuration allowed selective area metallizations without interrupting the ultra high vacuum grown environment. This arrangement frees the metal-semiconductor interface from the GaAs surface state contributions to Fermi level pinning arising from chemical contamination, cleavage steps, or sputter cleaning/anneal operations[111,112] encountered in the conventional fabrication of Schottky barriers. An outgrowth of the in situ deposition technique may provide a reliable procedure for realizing practical GaAs MOS devices.

6.2 SYSTEM CONFIGURATION FOR IN SITU DEPOSITIONS

Several modifications were incorporated in the basic MBE system for

the Schottky barrier studies. A schematic diagram of the modified system is shown in Figure 46. Installing the metal evaporator in the interlock chamber greatly enhances system flexibility without compromising the cleanliness of the GaAs growth chamber. It is significant that the experimental arrangement and processing sequence permits the measurement of Schottky barrier heights on a single epilayer exposed to several different ambients.

6.3 EXPERIMENTAL TECHNIQUE

Two micron thick GaAs epilayers were grown under As-stabilized conditions on (001) n^+-substrates held at 560-600 °C. The layers were intentionally doped n-type (3×10^{15} to 10^{17} cm^{-3}) by growing in the presence of a molecular beam from doping ovens loaded with either tin or germanium. Most of the samples were doped with Sn. This element segregates during MBE leaving a thin layer a few Å thick of unincorporated Sn at the outer surface[98,113]. The segregation can be reduced by increasing the As/Ga ratio during growth[99]. In the present study As/Ga ratios were approximately 100 and an Auger examination showed Sn was below the detection limit of 0.01 monolayer. Two layers were doped with Ge, a dopant which shows little tendency to segregate in MBE[18].

Following the epilayer growth, an As face was generated[14,111,114] by lowering the substrate temperature to 135-160 °C in an As atmosphere of 5×10^{-7} Torr. The sample was then withdrawn into the interlock chamber for metallization. After 30 minutes, the pressure was 2×10^{-8} Torr or less and the first metallization was applied to the heated substrate using a previously outgassed load wound on stranded W or Ta filaments*. The Ta filament was used to evaporate Ag. The substrate heater was turned off

*A Mo crucible was employed for MBE A0309.

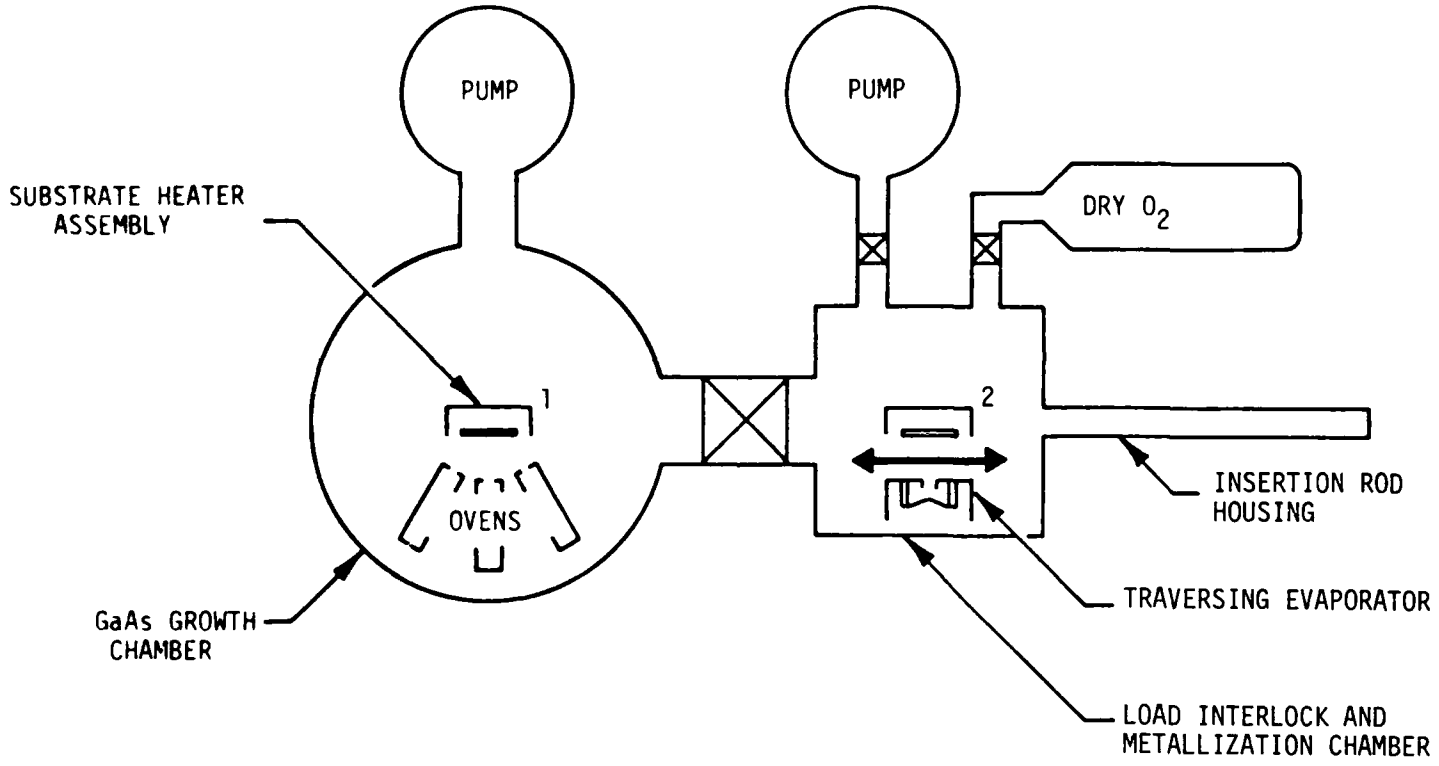


Figure 46. Schematic Diagram of MBE System Configured for Schottky Barrier Studies. After Growth of the Epilayer, the Substrate Heater Assembly is Moved from Station 1 to Station 2 for Multiple Metallization Depositions.

and the interlock chamber was opened to dry O_2 at a pressure of one atmosphere for 30 minutes. A second metallization was selectively deposited. The sample was transferred to a liquid nitrogen-trapped, diffusion pumped vacuum system for the third metallization. Arrays of Schottky diodes with diameters of 5 or 6 mils were defined over the three metallizations. A summary of the overall processing sequence is given in Table 10.

Table 10. Sequence of Processing operations for Schottky Barrier MBE Samples

- grow 2.0 μm n-GaAs layer under As-stabilized conditions
- selectively deposit 500-1000 Å metallization, T_{sub} ~ 135 °C
- introduce dry O_2 at one atmosphere for 30 minutes (in situ oxidation)
- selectively deposit 500-1000 Å metallization, T_{sub} ~ 27 °C
- transfer specimen to external diffusion-pumped evaporator (ambient oxidation ~ 15 minutes)
- selectively deposit 500-1000 Å metallization, T_{sub} ~ 27 °C
- define Schottky diodes (5.0 or 6.0 mils diameter) using conventional photolithographic techniques

Barrier heights for the diodes were computed by measuring the voltage intercept V_i taken from plots of $1/C^2$ versus bias voltage[115]. Approximately 12 capacitance values were recorded on a Boonton 75D capacitance meter in the interval $0 < | V_{bias} | \leq 3.0$ V. A correction for series resistance was applied in determining the junction capacitance at each bias voltage (Appendix I). In most cases the corrections were quite small (on the order of 0.01 percent), however, in situ Al diodes formed on layer MBE A0718 had low Q's ($3 < Q < 7$) and the capacitance corrections were 3-10 percent.

It is well known that anomalous barrier heights can be returned by

nonlinear $1/C^2$ versus V plots arising fron nonuniform doping, traps, inversion layers, etc[109,116-122]. The experimental data were fitted using a least squares method to a linear expression $y = ax + b$ where $y = 1/C^2$ and $x = V$. The coefficient of determination r^2 is a measure of the correlation between the experimental data and the linear expression. For an exact fit, $r^2 = 1$. Data yielding values of $r^2 < 0.9992$ were rejected in the present investigation.

Representative examples of the experimental data are shown in Figure 47. The different slopes indicate a distribution of doping concentration over the specimen (1.27×10^{17} cm^{-3} and 9.50×10^{16} cm^{-3} for the diodes in Figure 47). The doping concentrations are expressed in terms of these slopes by[115]

$$N_d = \frac{2}{q\varepsilon_o\varepsilon_r A^2 \frac{d(1/C^2)}{d(V)}} \qquad (21)$$

where

q = electronic charge,

ε_o = free space permittivity,

ε_r = GaAs dielectric constant[123] = 12.94, and

A = diode area.

The doping concentration fixed the position V_δ of the Fermi level with respect to the conduction band and therefore the barrier height ϕ_B could be expressed as[115]

$$\phi_B = V_i + V_\delta + \frac{kT}{q} - \Delta\phi \qquad (22)$$

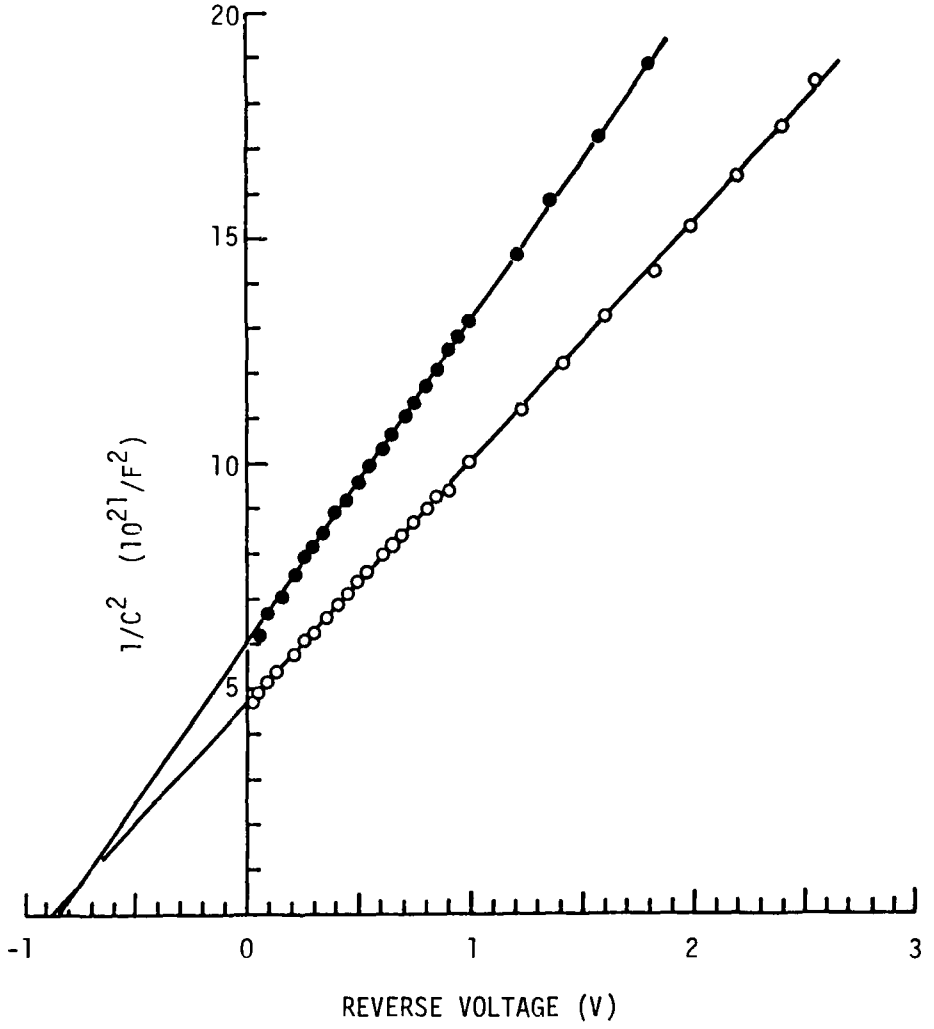


Fig. 47. Comparison of $1/C^2$ vs V Plots for Au-Schottky Barriers Formed in situ (●) and on an Oxidized Surface (o) of GaAs layer MBE A 0309.

where k = Boltzmann constant,

T = temperature, and

$\Delta\phi$ = image force lowering[67].

Completing the calculations in Equation 22 for the data shown in Figure 47 yielded barrier heights of 0.858 and 0.878 volts for the in situ gold and the oxide layer interfaces, respectively. Barriers of 0.95 volts have been obtained by differential capacitances measurements on gold Schottky diodes on vacuum cleaved GaAs surfaces[106].

6.4 ANALYSIS OF BARRIER HEIGHT MEASUREMENTS

Table 11 gives the average barrier height ϕ_{Bn} for Schottky barriers formed on the surfaces of eight MBE layers exposed to different ambients. There were four deviations from the processing sequence which led to inapplicable ϕ_{Bn} data at certain steps for layers A0309, A0505, and A0710.

Several conclusions can be drawn from the data in Table 11.

1. Schottky barrier heights for in situ metallizations on freshly grown MBE layers are lower than ϕ_{Bn} for oxidized surfaces. Low barrier heights of 0.6 eV for Ag (ion cleaned/annealed GaAs) and 0.66 eV for Al on As-stabilized surfaces have been reported by other laboratories[111,124]. In the case of layer MBE A0309, excessive outgassing was observed on the RGA during the in situ evaporation from a Mo crucible. It is likely that the relatively small difference between ϕ_{Bn} values for MBE A0309 arises from this contamination. Smaller pressure increments of typically 2×10^{-8} Torr (2×10^{-7} Torr observed in two instances) were obtained for the remaining depositions. There is little evidence

Table 11. Barrier Heights Measured for Schottky Diodes formed on MBE GaAs Layers Exposed to Different Ambients

Layer	Dopant	Concentration	Schottky Metal	Barrier Height			r^2_{min}
				ϕ_{Bn}(a)	ϕ_{Bn}(b)	ϕ_{Bn}(c)	
		(cm^{-3})		(±0.01 eV)	(±0.01 eV)	(±0.02 eV)	
A0309	Sn	10^{17}	Au	.86*	na	.88	.9996
A0419	Sn	3×10^{16}	Au	.83	.83	.86	.9998
A0505	Sn	$3\text{-}5 \times 10^{16}$	Au	.82	na	na	.9999
A0517	Sn	$3\text{-}7 \times 10^{15}$	Au	.81	.80	.88	.9996
A0519	Sn	3×10^{16}	Al	.55	.77	.68	.99998
A0525	Sn	3×10^{16}	Ag	.81	.82	.90	.9995
A0710	Ge	2×10^{16}	Au	na	.75	.83	.9996
A0718	Ge	$5\text{-}9 \times 10^{16}$	Al	1.10	.71	.68	.9992

(a) in situ Schottky

(b) in situ oxide + in situ Schottky

(c) Schottky deposited in diffusion pumped system after ambient oxidation

r^2 coefficient of determination

* H_2O contamination (1.2×10^{-6} Torr) observed during Schottky deposition

na not available

that alloying effects associated with in situ evaporations on substrates held at 135 °C are influencing the barrier height data in view of the extended time (on the order of hours) and higher temperatures ($\geq$ 200 °C) requ.red to observe changes in barrier heights for Al and Au on GaAs[109,125-127]. An increase in ϕ_{Bn} following surface oxidation is well documented[128-130]. The As-stabilized surface of GaAs is less susceptible to oxidation than the Ga-stabilized surface[14,131], and this is generally reflected in Table 11 as a small change in ϕ_{Bn} for the in situ oxidation. The oxidation pressure and time of exposure were sufficient to completely saturate dangling surface bonds[14,132]. Ambient oxidation which included exposure to water vapor as well as condensable pump vapors was much more effective in increasing ϕ_{Bn} for Ag and Au, but not for Al.

2. There is limited evidence that the surface state density is less for the in situ Schottky barriers than for barriers which include the oxide interface. Following Cowley and Sze the density of states D_s is written as[133]

$$D_s = \frac{\varepsilon_i}{q\delta}\left(\frac{1-\gamma}{\gamma}\right) \qquad (23)$$

where ε_i = dielectric permittivity,

q = electronic charge,

δ = interfacial layer thickness, and

γ = slope of the barrier heignt (ϕ_{Bn}) versus work function (ϕ_m) characteristic.

A practical difficulty encountered in determining D_s from

experimental ϕ_{Bn}, ϕ_m data lies in the extablishing values for ϕ_m[107]. For example, older references show low values for readily oxidized materials like Al (3.74 eV) that disagree substantially with more recent data (4.13 eV for Al)[134]. The data in Table 11 indicate that the in situ barrier heights are lower and γ is larger than the values measured by Spitzer and Mead for Schottky barriers deposited on vacuum-cleaved n-type GaAs[135]. It is known that the high density of surface states for the latter are dominant factors in pinning the Fermi level position at the surface independent of the metal's work function.

3. In contrast to the Au and Ag results, Al Schottky barrier heights on the in situ oxidized surfaces were actually 0.03 - 0.09 eV higher than those for surfaces exposed to ambient oxidation. The thin oxide loosely bound to the As-stabilized surface in the former case may have been reduced to form an interfacial layer of Al_2O_3 which increased the magnitude of ϕ_{Bn}. The process appears to be less effective for surfaces exposed to the in situ plus ambient oxidation.

4. Special mechanisms are required to understand the low diode Q and high barrier height (1.1 eV) for the in situ Al Schottky diodes for MBE A0718. As noted below, the demonstration of epitaxy rules out the possibility of surface contamination prior to metallization. The in situ contacts may have been thin. Under these conditions, the barrier height could be influenced by contamination from the photolithographic process or by series resistance in the Schottky metallization (smaller C-V variation

and larger V_i)[135].

Finally, it is important to note that a preliminary RED analysis indicates that the growth of the in situ Al on MBE A0718 was epitaxial. Following the 30 minute oxidation, the RED pattern from the second Al metallization changed to a ring structure characteristic of polycrystalline growth. The observation of epitaxial Al growth is not unexpected. Other laboratories have recently reported Al and Ag epitaxy on (001) surfaces of GaAs and InP[13,124,136,137]. The epitaxial growth of Al raises the possibility that a low surface state density may be achieved at the interface between an anodized Al layer and a GaAs epilayer.

6.5 MOS INVESTIGATION

There is presently considerable interest in identifying an insulator with good dielectric properties that will eliminate Fermi level pinning at GaAs surfaces. The dielectric properties of conventional thermal oxides[138] are unsuitable for use in MISFET applications, and the relatively high temperatures (several hundred °C) involved in depositing silicon oxides, silicon nitrides or silicon oxynitrides induce surface vacancies which lead to pinned Fermi levels[139]. Defect vacancies are also observed in conventional anodic processing techniques. In MBE the character of the freshly grown surface can be defined with precision and freedom from impurity contamination. Recent attention has focused on the post deposition of Al_2O_3 layers using oxygen gas/Al molecular beams[140] and thin AlAs layers which were later oxidized thermally[141]. An alternative approach has been investigated in the Georgia Tech MBE system.

Following the growth of a 2.0 μm thick epilayer, the specimen was withdrawn into the interlock/metallization chamber for deposition of a 150 Å

thick Al film. The investigation includes both n- and p-type epilayers grown on n^+- and p^+- substrate, respectively. The Al film thickness is controlled by a quartz monitor attached to the traversing evaporator. The samples are subsequently anodized and processed into MOS structures. Material and electrical characterizations of the dielectric/GaAs interface are in progress.

7.0 FABRICATION AND EVALUATION OF MICROWAVE AND MILLIMETER WAVE DEVICES

A number of device structures were fabricated and evaluated to further assess the potential of MBE materials for achieving the control of doping profiles and quality of material which are basic prerequisites for high performance microwave and millimeter wave devices. The structures investigated on this phase of the program included mixer diodes, FETs, IMPATTs and hyperabrupt varactors.

7.1 MILLIMETER WAVE MIXER DIODES BY MBE[142]

MBE layers were grown on low resistivity Si doped substrates for the fabrication of mixer diodes. The material was grown with a 1.0 μm thick Sn doped (1-2 x 10^{18} cm^{-3}) buffer layer and active regions 0.2 - 0.3 μm thick with Sn doping between 1-6 x 10^{17} cm^{-3}. The layers were grown without interruption and the doping level changed by reducing the Sn oven temperature from 650 °C to 550 °C. The substrate temperature was held at 540 °C during growth of the active layer. With this method the sharpness of the interface between layers is determined by the growth rate (0.9 μm/hr) and the thermal response of the Sn oven (2-3 min.). Profiles for two layers are shown in Figure 48 using the doping profiler and the point by point C(V), Q(V) method described in Appendix I. The Schottky diodes for these measurements were 3 mil diameter gold dots. Nonphysical results are returned by the profiler near the interface between the active and buffer layers.

After the epitaxial growth process, the wafers were coated with 0.4 μm of SiO_2 by chemical vapor deposition. An array of 2.0 μm diameter holes was etched in the oxide and Schottky barrier diodes were formed by electroplating gold through the holes. Figure 49 is a SEM photograph showing an

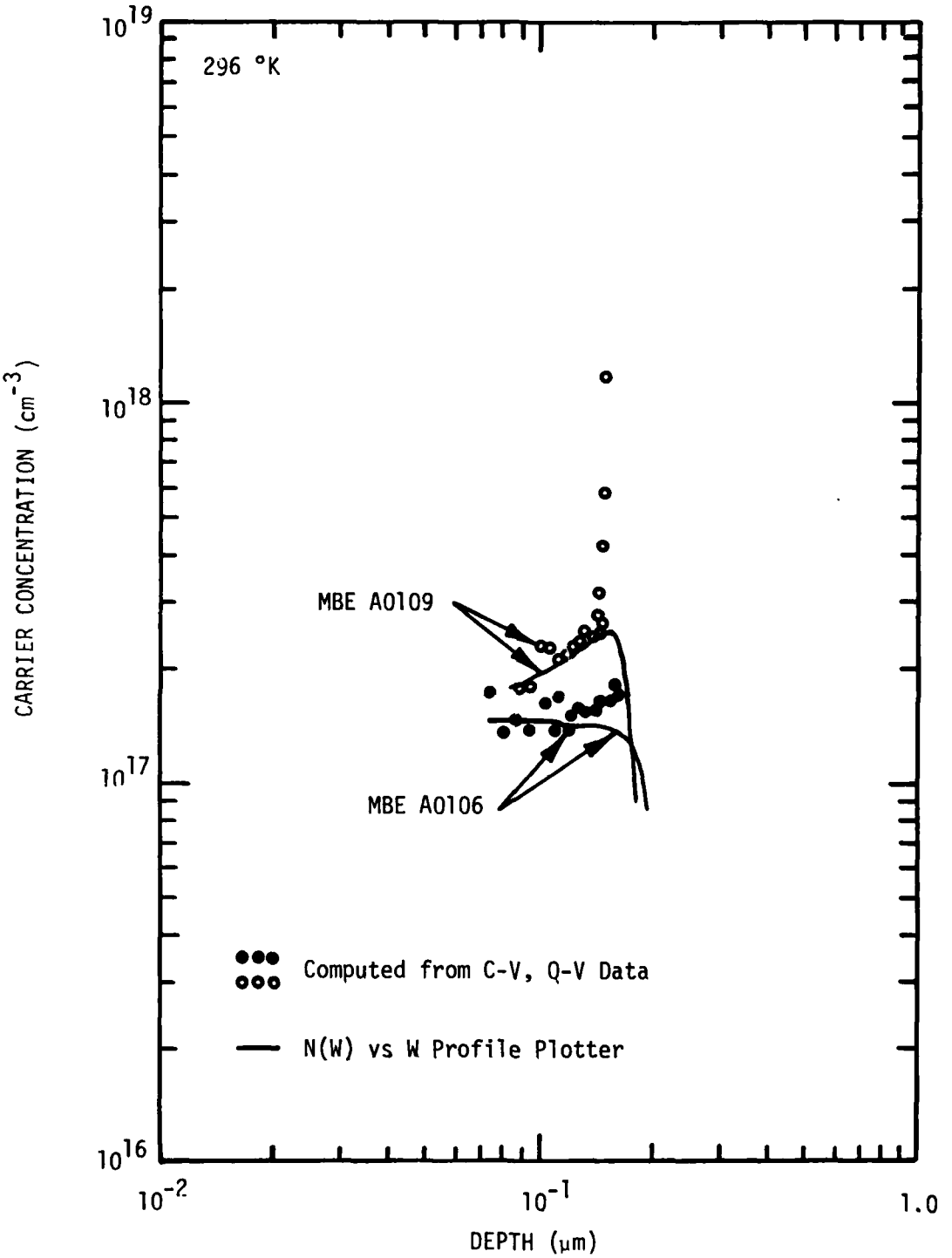


Figure 48. Doping Concentration Profiles for Sn-Doped GaAs Used in Mixer Diode Fabrication.

Figure 49. Two micron Diameter Holes Etched in Oxide to Define Mixer Diode Area.

array of holes in the oxide before electroplating. A cross sectional drawing of the diode construction is given in Figure 50. The substrate material was thinned to 50-60 μm by chemo-mechanical polishing with sodium hypochlorite. Metallization for substrate contact, scribing and breaking complete the fabrication process up to the packaging stage.

Packaging of the die varied according to the r.f. test frequency and particular requirements of the laboratory involved in the r.f. testing and evaluation. The die packaged at Georgia Tech were solder bonded and contacted in the package with a W whisker. Die for r.f. testing at 35 GHz were mounted in a ceramic microwave package modified for the tungsten whisker contact. For higher frequency testing, the die were mounted and contacted in Sharpless wafers.

Packaged devices have been tested and evaluated at 35 GHz and 92 GHz. The double sideband noise figure for seven devices was measured at 35 GHz by W. Baldwin Day in a test set up at Sperry Microwave Electronics in Clearwater, Florida. The data for the MBE devices are given in Table 12 along with other diodes purchased from commercial vendors. Diodes one and two listed in the table are the diodes in the balanced mixer. Comparative noise figures are obtained by substituting the test diode for one of the diodes in the balanced mixer. The best of the MBE diodes performed as well as the best of nearly 300 commercially available diodes tested in the same setup. Measurements of the d.c. characteristics give series resistance between 7-16 Ω and quality factors of 1.1 to 1.3. Figure 51 shows the forward I-V characteristics of the diode that gave the best r.f. performance. Measurements at 92 GHz were made here at Georgia Tech using a single diode mixer. Several diodes were tested and the double-sideband noise figure was

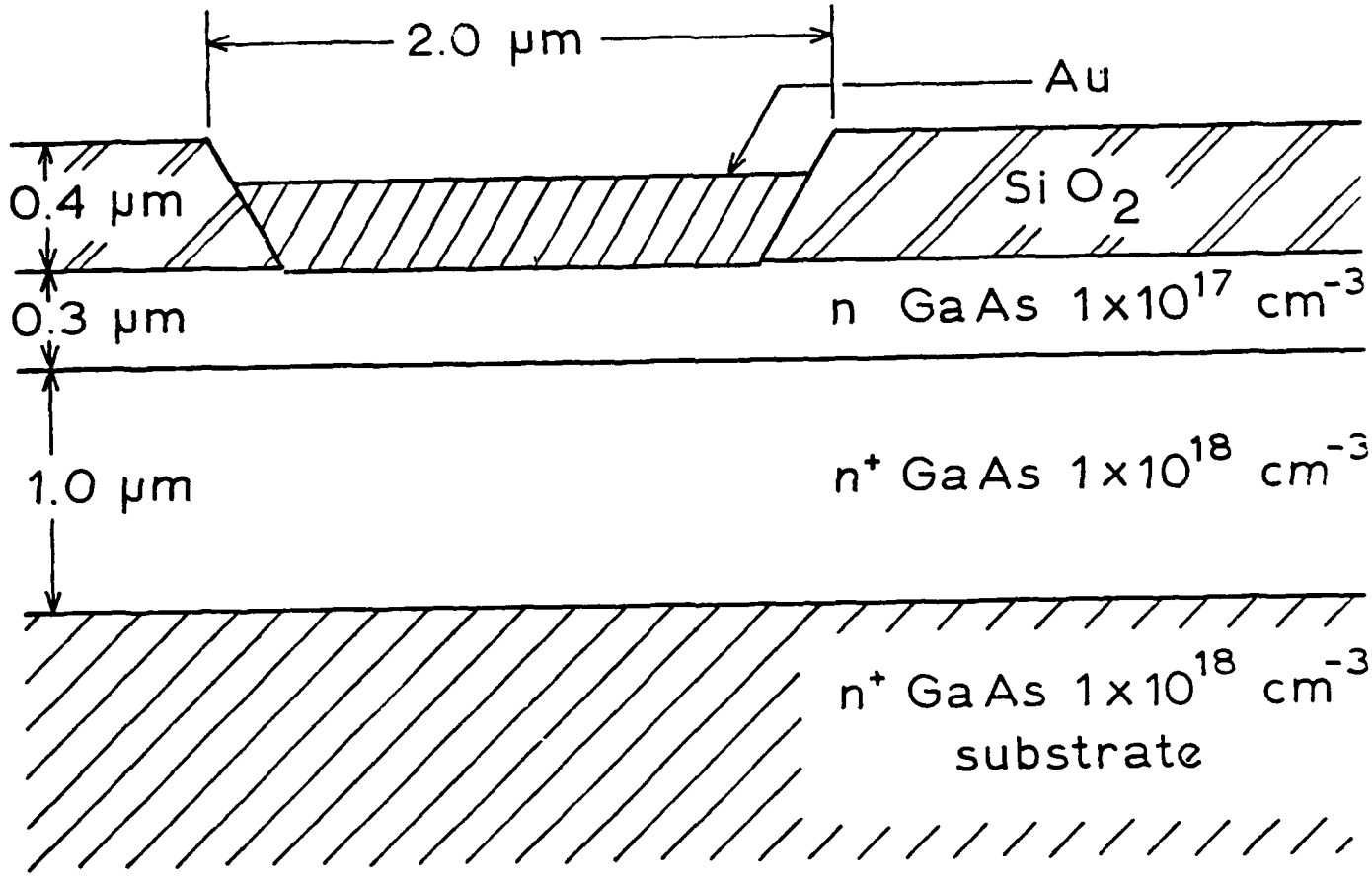


Figure 50. Schematic of MBE Mixer Diode Construction

Table 12. Test Data for MBE Mixer Diodes

Diode 1	Rs Ω	Quality Factor	Diode 2	Noise Figure dB	Conversion loss dB
MBEA-1-2	14	1.18	TRG-2	5.95	6.65
-1-3	10	1.10	TRG-2	5.80	6.50
-1-4	16	1.13	TRG-2	6.08	6.78
-1-5	9	1.12	TRG-2	5.60	6.30
-1-6	8.5	1.30	TRG-2	6.20	6.90
-2-1	7.5	1.15	TRG-2	5.70	6.40
-2-3	8.2	1.10	TRG-2	5.25	5.95
MBEA-1-5			MBEA-2-3	5.15	5.85
TRG-1			TRG-2	5.60	6.30
CG71-3-222			CG71-3-223	4.85	5.55
MBEA-2-3			CG71-3-223	4.85	5.55

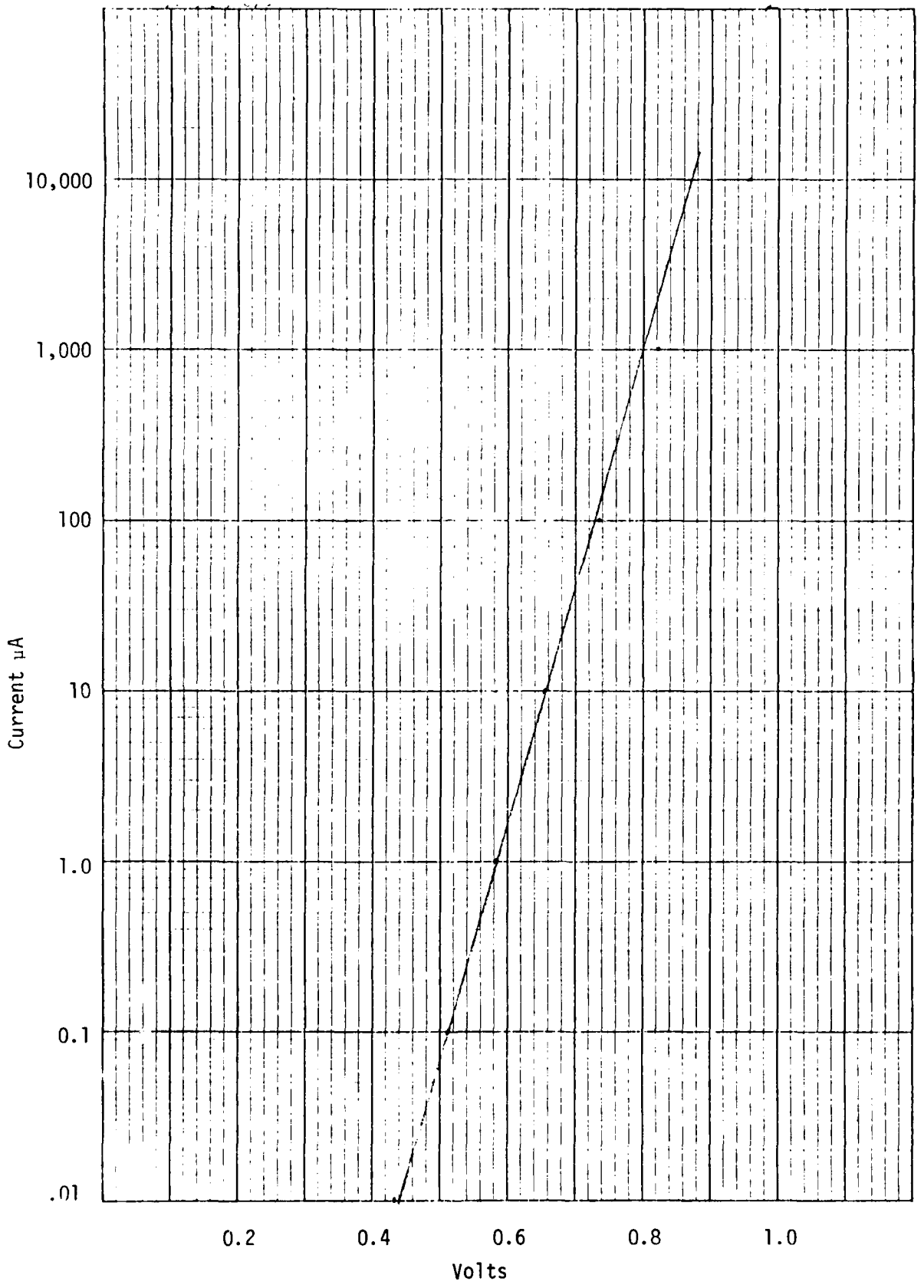


Figure 51. Forward I-V Characteristics of Diode MBE A-2-3

typically 8.3 db.

Tin was initially employed as the n-type dopant for MBE mixer diodes. However, yield problems have been encountered in growing subsequent layers with mixer profiles. Only three out of twelve layers showed series resistances of 10 ohms or less. The high series resistances found in the remaining samples are associated with two problems arising from Sn-doping of buffer layers; namely, a low overall doping concentration and an unintentional drop in doping level near the substrate-buffer interface.

Table 13 summarizes the growth parameters and doping concentrations experimentally measured for several buffer layers. With the exception of MBE A0601, the Sn-doped layers exhibited high series resistances.

Table 13. Growth Parameters and Doping Characteristics for Mixer Diode Layers.

Diode	Dopant	$T_{substrate}$ (°C)	$T_{n\text{-}oven}$ (°C)	Step Depth i(μm)	Step Depth j(μm)	Doping Concentration $N_i(cm^{-3})$	Doping Concentration $N_j(cm^{-3})$
MBE A0316	Sn	600	630	0.58	0.85	$2.7x10^{17}$	$1.4x10^{17}$
MBE A0524	Sn	605	690	0.48	1.04	$4x10^{17}$	$2.3x10^{17}$
MBE A0531	Sn	540	670	0.64	1.00	$2.5x10^{17}$	$1.6x10^{17}$
MBE A0601*	Sn	520	710	0.59	1.05	$7x10^{17}$	$8x10^{17}$
MBE A0620	Ge	557	860	0.55	1.08	$3.5x10^{18}$	$2.2x10^{18}$

*0.2 monolayer Sn predeposited before growing buffer layer; R_{series} nonuniform.

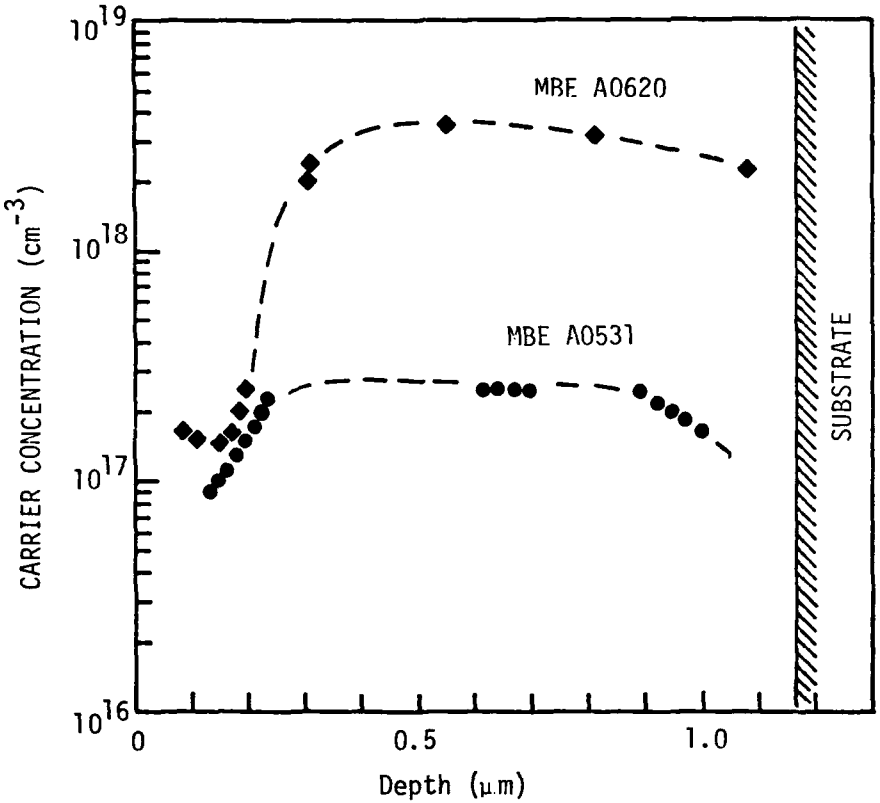
The carrier concentrations were obtained from C-V data for 3.0 mil gold Schottky diodes formed on steps which were successively etched into the epilayers using a weak Br-methanol etch (1:700). At room temperature, the solution etched (001) GaAs at the rate of 0.25 to 0.28 μm min^{-1}. Not only

is the buffer layer doping lower than targeted, there is evidence in Table 13 that the Sn-doping actually decreases near the buffer layer-substrate interface. The ratio N_i/N_j is largest at the highest substrate temperatures. As shown in the composite doping profile for MBE A0531 plotted in Figure 52(a) the doping gradient at the interface can be considerable. The forward I-V characteristics for Schottky diodes formed on this material are given in Figure 52(b), and it is clear that MBE A0531 is quite inadequate for mixer applications. In contrast to the Sn-doped layers, the Ge-doped specimen (MBE A0620) featured high doping in the buffer layer and a series resistance of approximately eight ohms. The deepest data point may in fact correspond to the substrate doping level since the accuracy of the chemical etch rate is no better than 10 percent.

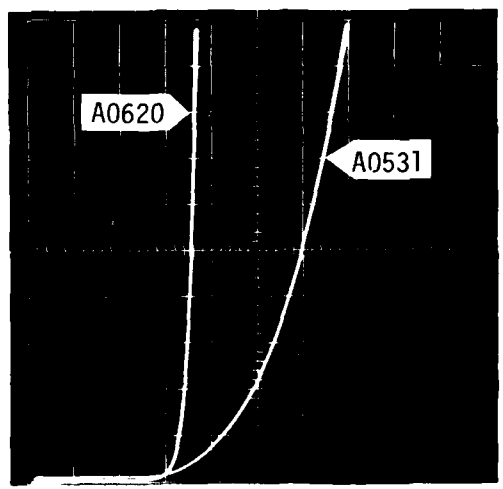
Potential problems are identified with the use of Sn as an n-type dopant in fabricating low noise GaAs mixer diodes. Tin tends to segregate, particularly during the initial stages of growing heavily doped layers of MBE. In an electron probe analysis of MBE A0524, tin was observed at the level of 50 ppm which is higher than the electrically active doping concentration. Auger studies indicate that the tin concentration within a few monolayers of the outer surface can be some three orders of magnitude larger than the level in the bulk of the layer[98]. Factors which reduce tin segregation include growing at substrate temperatures below 500 °C, doping at lower concentrations, predepositing Sn on the cleaned substrate, and increasing the As_4/Ga flux ratio[98,99]. Germanium appears to offer better doping control in the 10^{18} to 10^{19} cm^{-3} range required for n^+-buffer layer applications.

7.2 MBE MATERIAL FOR FET

Material for FETs was prepared by growing a 1.0 μm thick unintentionally



(a)



1.0 ma cm^{-1}; 0.2 V cm^{-1}

(b)

Figure 52. Electrical Characteristics of GaAs Mixer Material Doped with Sn (MBE A0531) and Ge (MBE A0620). The Gold Schottky Diodes Formed on the Layers Had Diameters of 3.0 mils. (a) Doping Profiles; (b) Forward I-V Characteristics.

doped buffer layer on semi-insulating substrates then opening the Sn oven shutter to continue growth of 0.2 μm thick active region doped at 2×10^{17} cm^{-3}. Several layers were grown with these target parameters for d.c. evaluation at both NRL and Tech. The r.f. evaluation of devices made from this material is in progress.

Devices were successfully made from samples A0404 and A0405. Aluminum Schottky barrier gates were used and ohmic source/drain contacts were made with Au:Ge with a thin Ni top layer to prevent balling-up during alloying. A folded geometry was used as shown in Figure 53. The gate width was 157 μm for each side; the gate length was 3 μm; and the source drain separation was 9 μm. Devices near the edge of sample A0404 exhibited I-V characteristics as shown in Figure 54. The transconductance of this device was found to be 1.0 millimho at V_{ds} equal to 3.0 volts. The characteristics of the Schottky barrier gate and the ohmic drain-source contacts are also shown in Figure 54 Not all areas of the sample yielded functional devices, and in many cases, FETs burned out or characteristics changed during testing. We have not been able to determine the cause of the nonuniformity for different regions of the sample or for the "tenderness" of the devices. Sample A0405 was processed in a similar way and the characteristics of the devices made from this material are shown in Figure 55. For this device, a transconductance of 4.2 millimhos at V_{ds} equal to 3.0 volts (one side of the folded geometry) was obtained.

A large difference in the impurity profile taken at different parts of A0404 has been noted. Figure 56 shows profiles taken at Tech and NRL from different parts of the sample. An impurity spike in the buffer layer was observed on one of the profiles taken at NRL. These differences in the profile could account for the observed nonuniformity in devices across the sample

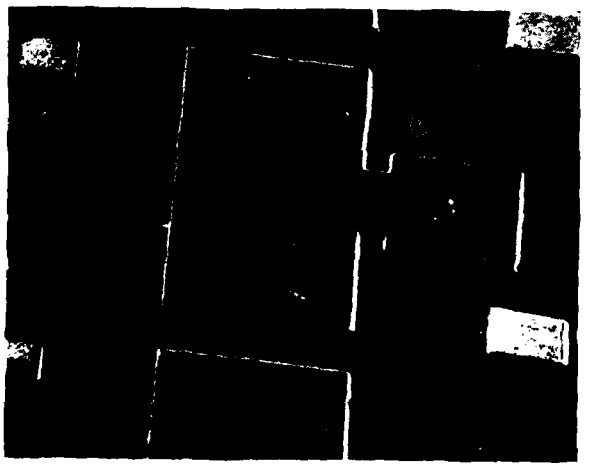
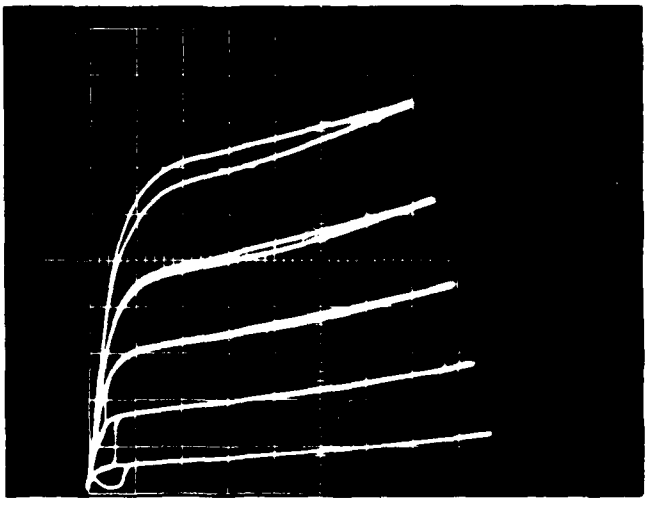


Figure 53. Geometry of FET Devices



1.0 mA/cm

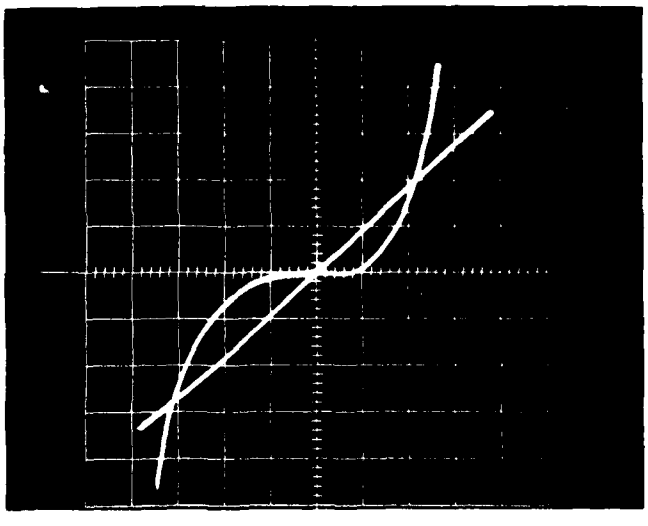
0.5 V/cm

0.2 V/step

Lower right corner of sample

Both sources connected

Vertical: Current
Horizontal: Voltage



Schottky

Reverse 0.05 mA/cm

10.0 V/cm

Forward 0.05 mA/cm

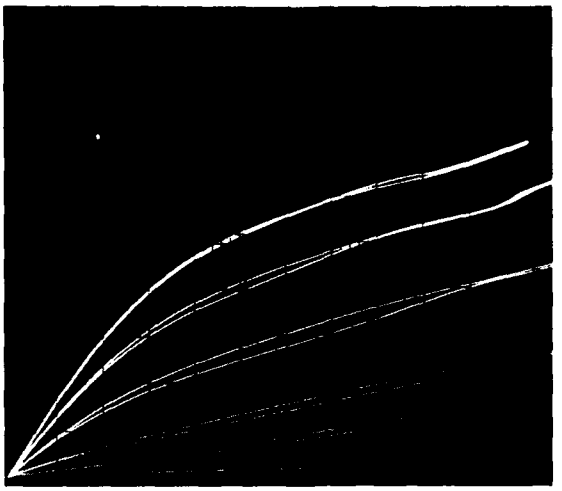
0.5 V/cm

Ohmic D-S

.1 mA/cm

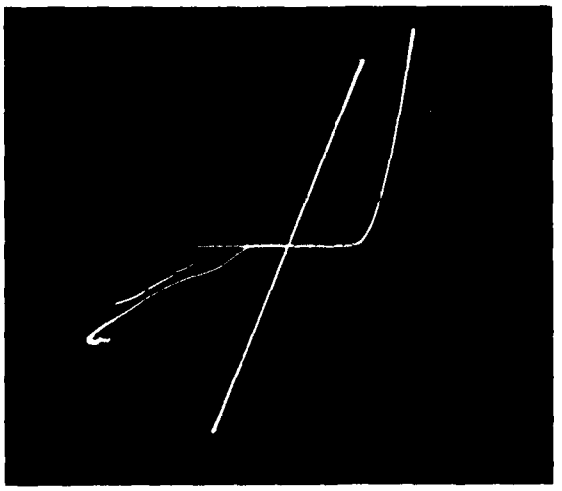
.05 V/cm

Figure 54. Characteristics of MBE A0404



V_{gs} = 0
.5
1.25
2.25
3.25
7.25

Vertical - 2.0 mA/cm
Horizontal - 0.5 V/cm



Ohmic
0.5 mA/cm
0.1 V/cm

Schottky
Forward 0.1 mA/cm
Reverse .1 mA/cm
5 V/cm

Figure 55. Characteristics of Sample MBE A0405

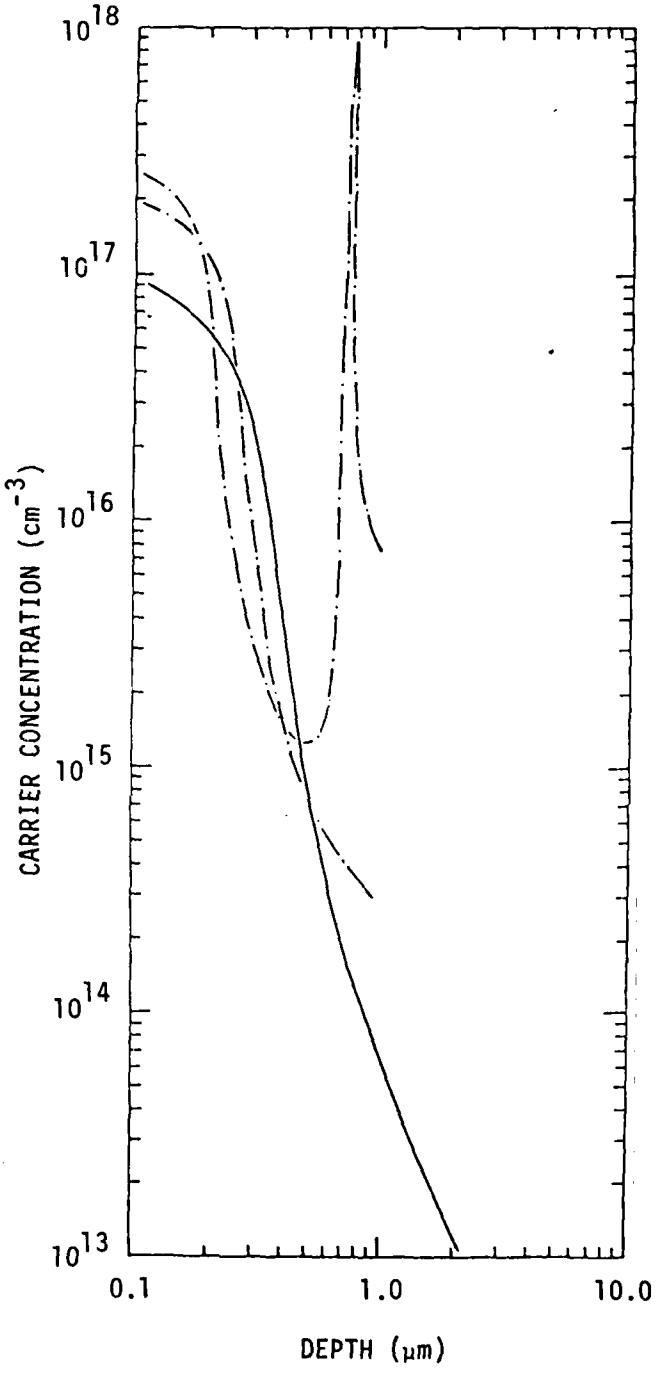


Figure 56. Doping Concentrations of Fet Structure MBE A0404 Measured at Georgia Tech (solid) and NRL (dash-dot).

as mentioned above, but the cause for the variation in the profile is not known. Due to the geometry of the system, the axis of the doping source is not perpendicular to the substrate but comes in at an angle. The angular source axis is expected to cause a gradual change in the impurity across the sample at any given depth into the grown layer. This does not seem to fit what has been observed and definitely does not explain a spike in the buffer layer that only occurs in part of the sample.

At present, it is suspected that the same problems with Sn doping as described above for mixer diodes are occurring in the preparation of the FET layers. Better control was obtained with Ge dopant for mixer diodes but no Ge doped layers were prepared for FET devices.

7.3 IMPATT DOPING PROFILES PREPARED BY MBE

High-low GaAs IMPATT materials have been grown for both Schottky barrier and grown p-n junction devices. Changes in the n-type doping level were made by adjusting the temperature of the n-type dopant oven. The p-type dopant (Be) was introduced by opening the p-type oven shutter and simultaneously closing the n-type oven shutter. The results of MBE A0321 indicate the sharp, abrupt changes in doping profiles required in IMPATT structures were not generated where Sn was used as the n-type dopant. A much more abrupt change was obtained in MBE A0816 when Ge was used as the n-type dopant. This is another example of the poor behavior of Sn for an n-type dopant. Figure 57 shows doping profiles for MBE A0816, MBE A0321, and a Varian[143] X-band pulsed GaAs p^+-n IMPATT device. Layer MBE A0816 shows the most abrupt high-low interface but breaks down before the entire profile can be obtained. This diode has a grown p-n junction and the profile was obtained for a 5.0 mil diameter mesa.

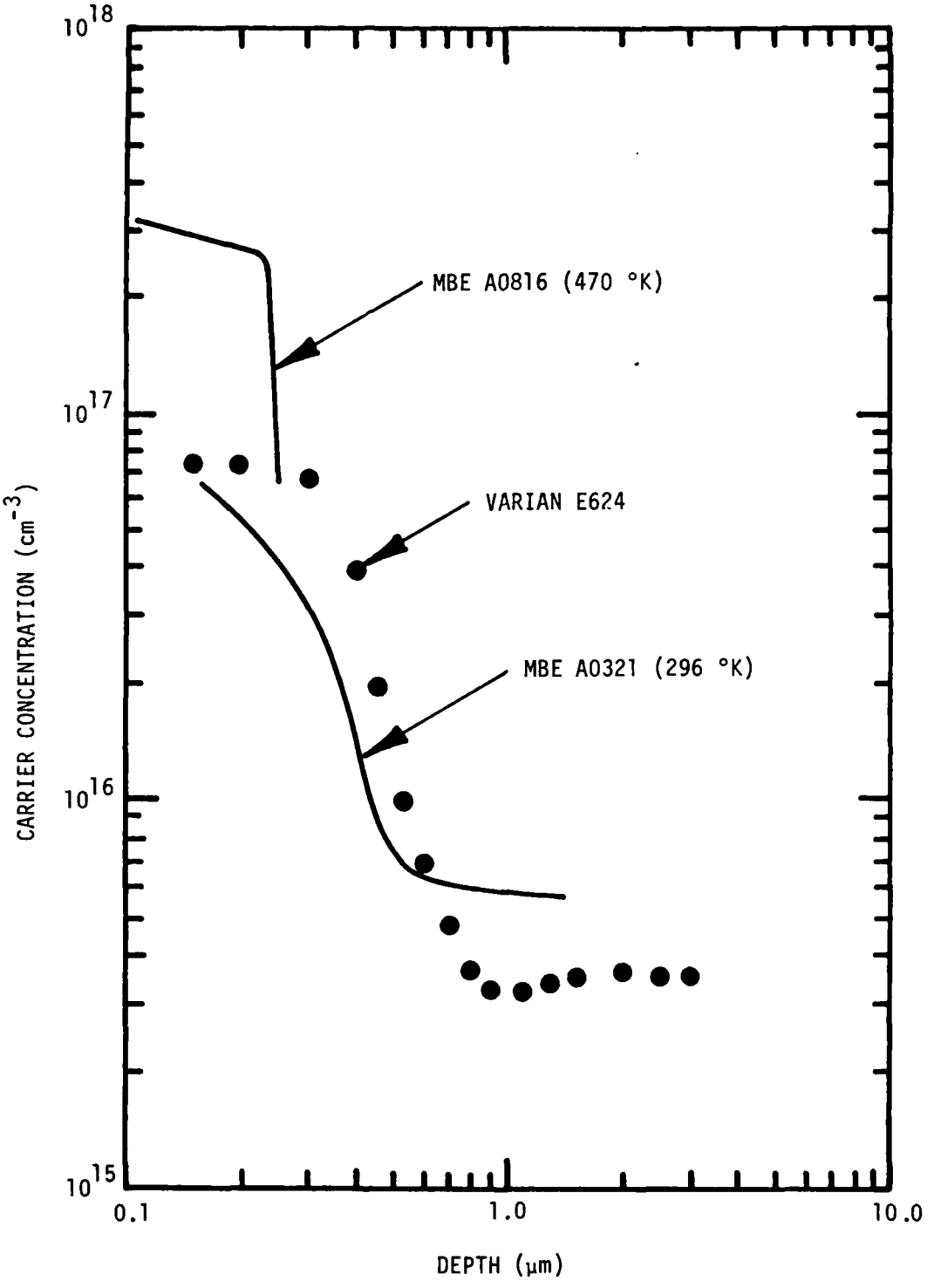


Figure 57. Doping Profiles of the High-Low Region of Schottky (MBE A0321) and p^+-n (MBE A0816, Varian E624) IMPATTs.

The data given above must be qualified in that the doping profiler cannot accurately reflect the abrupt changes in impurity atom profiles encountered in high performance high-low and low-high-low IMPATT structures. A concept which is useful in characterizing the widths of space charge regions in extrinsic semiconductor materials is the effective Debye length L [144].

$$L = \left(\frac{\varepsilon_r \varepsilon_o \, kT}{q^2 (n+p)} \right)^{1/2} \qquad (24)$$

where ε_r = dielectric constant,

ε_o = permittivity of free space,

k = Boltzmann constant,

T = temperature,

q = electronic charge,

n = electron density, and

p = hole density.

A plot of this expression for GaAs is given in Figure 58. With abrupt changes in impurity atom profiles, there is a distribution in the space charge region that extends over distances of approximately 6 L where L is computed for the more heavily doped region[145]. In this approximation an impurity spike 12 L wide would appear to have a half width of 6 L.

The IMPATT structures were prepared by growing a 1.0 μm thick buffer layer doped at greater than 10^{17} cm^{-3} on top of the Si-doped substrate. This was followed by a 5.0 μm thick drift region doped at 6×10^{15} cm^{-2} and a narrow step doped at a higher level. Injecting the high region using a second shuttered n-type oven would yield a sharper boundary which more nearly approaches the limits established by the space charge region for an

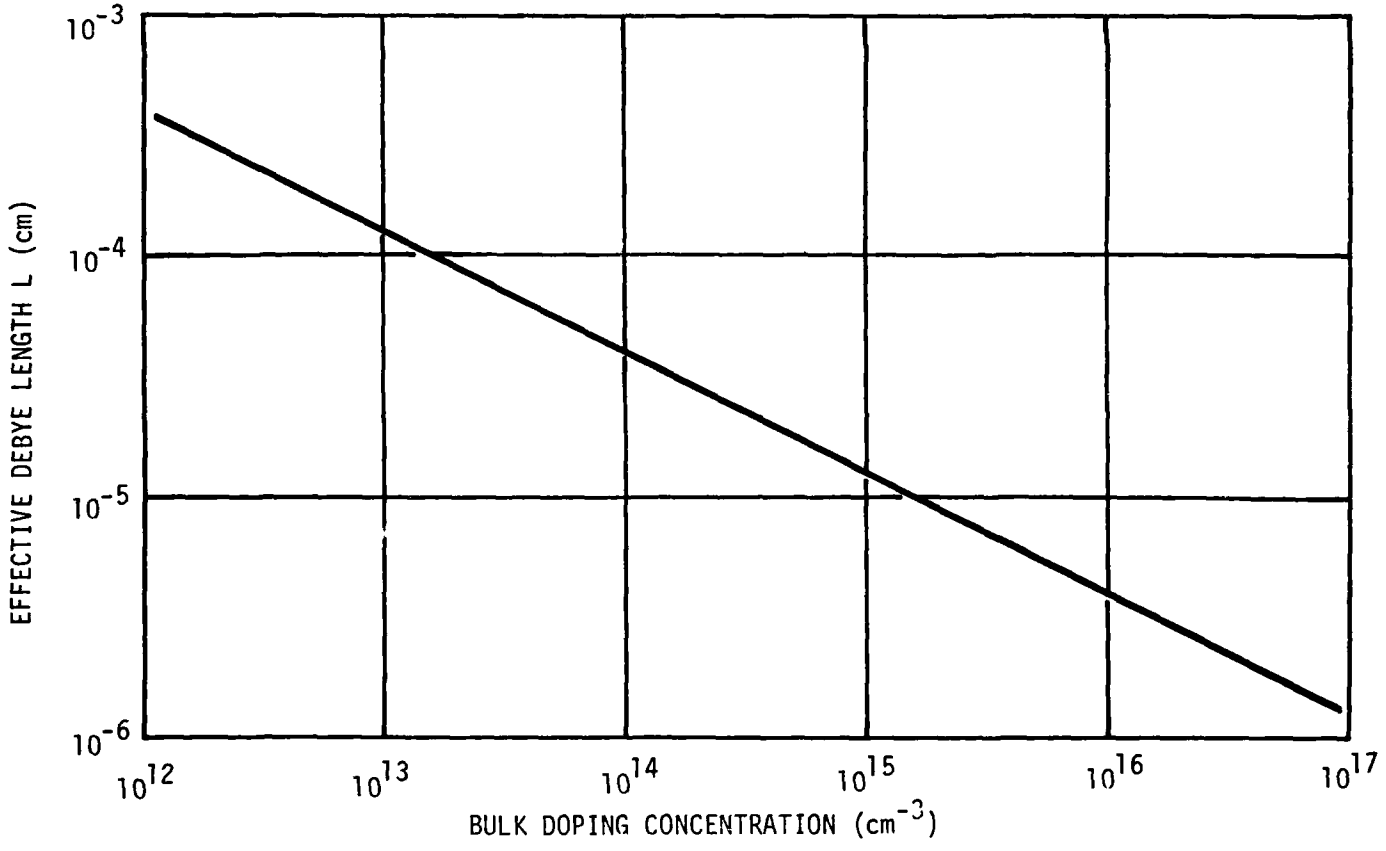


Figure 58. Effective Debye Length in GaAs as a Function of Bulk Doping Concentration

abrupt step.

7.4 p^+-n HYPERABRUPT GaAs VARACTORS

The design of hyperabrupt varactors for a given voltage dependence of capacitance involves careful tailoring of the doping profile in the depletion region. Precise doping control during MBE can be readily achieved by simply varying the rate of dopant deposition while holding the epi-layer growth rate constant.

In addition to the Ga and As ovens filled with 6N material, doping ovens were loaded with 6N Ge and 3N5 Be. The substrate temperature was held at 560 °C during the epi-layer growth at the rate of 1.0 μm hr^{-1}. The varactor construction consisted of an initial 1.0 μm thick n^+-buffer layer (2×10^{18} cm^{-3}) on a Si-doped (001) substrate followed by a 1.2 μm thick n-layer ($8 \times 10^{15} < N_d < 2 \times 10^{17}$ cm^{-3}) and a 0.8 μm thick p^+-layer (8×10^{18} cm^{-3}). The dopant type was selected by actuating mechanical shutters in front of the Ge (n and n^+) and Be (p^+) ovens. During the growth of the n^+- and p^+-layers, the temperatures of the Ge (850 °C) and Be (775 °C) were maintained at uniform levels. For the n-layer, however, the temperature controller of the Ge oven received an incremental adjustment every two minutes which gradually increased the oven temperature from 670 °C to 791 °C. Ohmic contacts were formed with Ni/Au(88%)Ge(12%) and Ag(82%)In(12%)Mn(6%) layers deposited on the n^+-substrate and p^+-epilayer, respectively. Conventional photolithographic techniques were used to define mesa diodes 152 μm in diameter.

The doping profile in Figure 59 was derived from C-V measurements taken on a Boonton 75D capacitance bridge. As the figure indicates, programming the temperature of the Ge oven yields a donor density $N_d \alpha x^m$ where $m \sim -1.2$

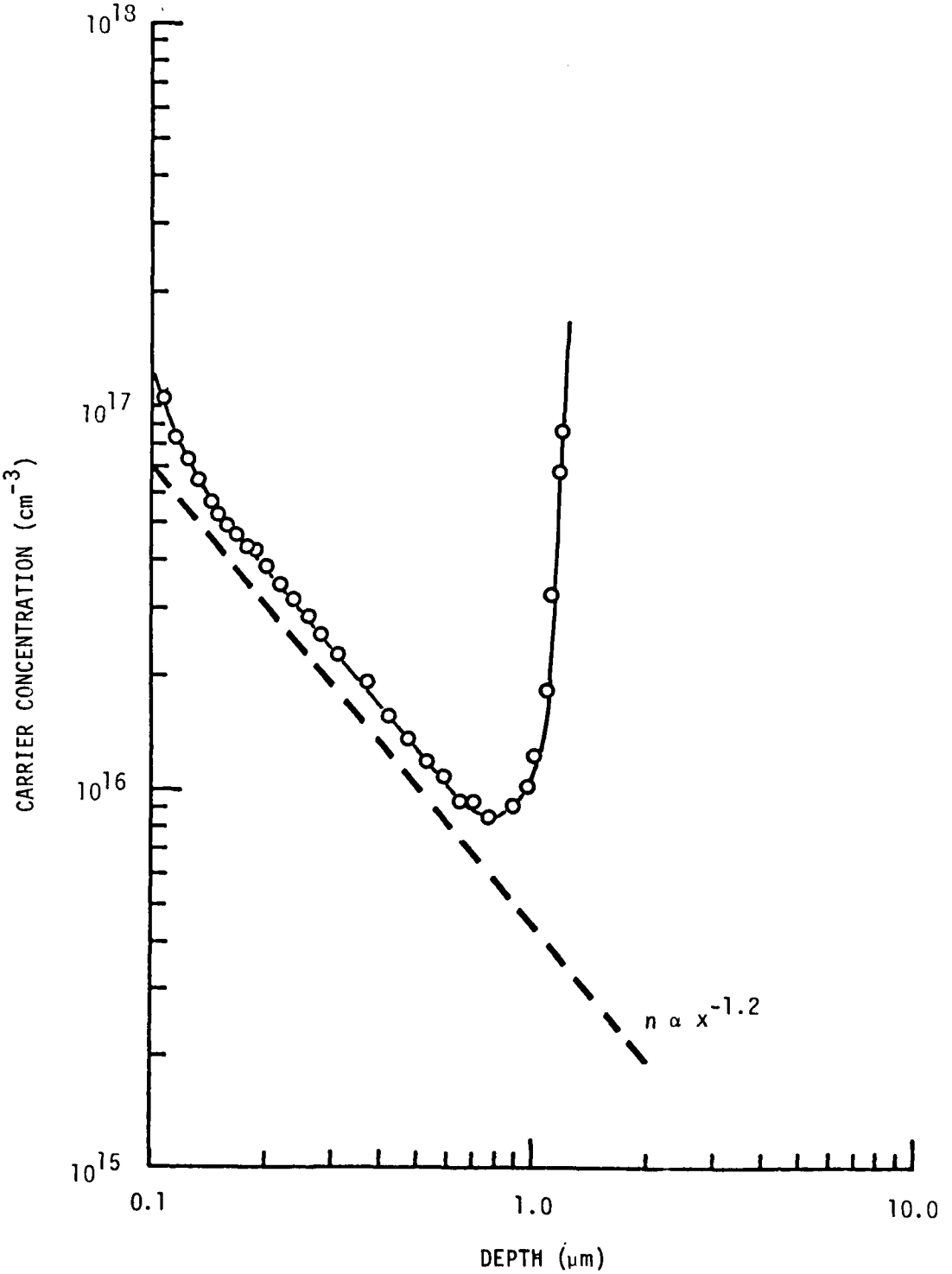


Figure 59. Doping Profile for Hyperabrupt p^+-n Junction GaAs Varactor Diode MBE A0821.

in this example. Other values of m ($-1.8 < m < 0$) have been demonstrated for Schottky barrier varactors fabricated with MBE[25].

Figure 60 shows the capacitance/voltage characteristic of the GaAs varactor. The diode capacitance varies from 20 pF to 2 pF as the bias voltage changes from zero to 12 V. The least squares fit to a straight line for a $C^{-1/n}$ vs. V plot in the range $-6 < V < -0.5$ occurs for the built-in voltage V_{bi} = 1.41 eV and n = 1.2. These data compare with V_{bi} = 1.38 eV and n = 1.25 based upon the given doping levels and a theoretical model[146] of a one-sided junction where $n = (m+2)^{-1}$.

The major contribution to series resistance R_s in a p^+-n hyperabrupt varactor arises from the undepleted portion of the n-epilayer. This component is expressed as $R_n = A^{-1} \int \rho_n(x)dx$ where A is the diode area and $\rho_n(x)$ is the layer resistivity. A statistical analysis of 11 n-type MBE layers spanning the doping range 1.3×10^{15} to 1.8×10^{18} cm^{-3} indicates that the following empirical relationship exists between ρ and n:

$$\rho = 1.865\ 10^{13}\ n^{-0.88865} \quad \text{(ohm cm)}. \qquad (25)$$

For the doping range indicated here, Equation (25) yields results that are similar to those obtained by a regression analysis of ρ vs. n data for GaAs at 300 °K given by Sze and Irvin:[94]

$$\rho = 4.5079\ 10^{13}\ n^{-.91104} \quad \text{(ohm cm)}. \qquad (26)$$

Equation (25) in conjunction with the profile given in Figure 59 yields $R_n \sim 1.30\Omega$ at zero bias for a 30 μm diameter diode. Using conventional techniques[147] a value of 0.76 ohms is estimated for the remaining contact, spreading, and p-layer (thinned to 0.2 μm) resistive contributions. Thus

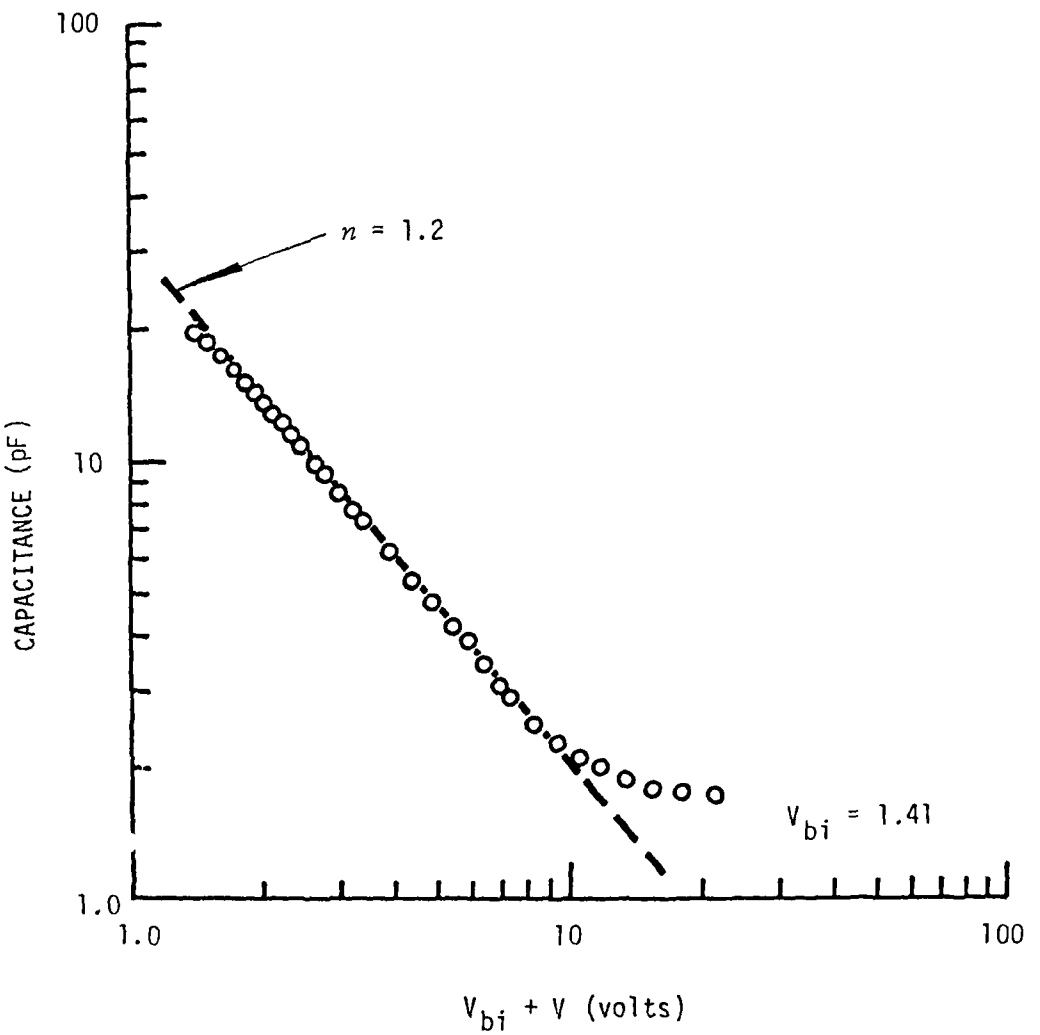


Figure 60. Capacitance/Bias Voltage Relationship for GaAs Hyperabrupt Varactor Diode MBE A0821

we project a zero bias cutoff frequency $f_{c0} = (2\pi R_s C_0)^{-1} \sim 99$ GHz where $C_0 = 20\ (30/152)^2 \approx 0.78$ pF.

8.0 GROWTH OF MBE GaAs ON (111) Ge

8.1 INTRODUCTION

Gallium arsenide epilayers were grown by MBE on Ge substrates to investigate the process and device potentials of peeled film FETs and mixer diodes. A preferential etch allows the selective removal of thin multi-layer GaAs device structures from the underlying Ge substrates. A high degree of epitaxy can be achieved for the GaAs growth[7,148-151] since Ge has an excellent lattice match to GaAs (0.07 percent at room temperature). In addition, the coefficients of thermal expansion for the two materials track closely.

Preliminary results of this investigation are reported below. The substrate cleaning procedures are given in Section 8.2. Details of the evaluation of the Ge substrates and the analysis of the GaAs epilayers are presented in Section 8.3.

8.2 SUBSTRATE PREPARATION

The following etches were evaluated on the "as-received" Ge wafers*.

1. CP4: 25 ml HNO_3 (69%), 15 ml CH_3COOH (99.9%), 12 ml HF (49%), 3 drops Br
2. CP8: 5 parts HNO_3, 3 parts HF, 3 CH_3COOH
3. WHITE ETCH: 3 parts HNO_3, 1 part HF
4. SUPEROXOL (modified): 20 parts H_2SO_4 (95-98%), 4 parts H_2O, 1 part H_2O_2 (29-32%), 1 part HF

The Superoxol etch was "rotated" with a magnetic spinner during etching; the others were not agitated. Both warm (i.e. 50 °C) and room temperature

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* Wafers were vapor degreased in Trichlorethylene before all etching operations.

etching was tried. Also, etches diluted with DI water were used; the White etch, for example, seemed to give a smoother surface when diluted with one part DI water. In many cases the etching seemed to enhance the surface features and reveal new ones such as scratches that were not visible on the original wafers. Chemical polishing of the as-received Ge wafers was tried using a 5.25% solution of NaOCL (Clorox) fed onto a cloth-covered polishing wheel. This technique will chemically polish GaAs wafers quickly, however, the Ge surfaces reacted slowly with the solution and the surface was not improved by this action.

8.3 SURFACE ANALYSES OF Ge SUBSTRATES AND GaAs EPILAYERS

Surface analysis methods included visual observation, electron diffraction (RHEED), and X-ray diffraction. Electron diffraction was employed in characterizing the surfaces of chemically etched Ge and the grown GaAs layers. The patterns were taken on an RCA EMU-3E microscope operating at 100 keV.

Figure 61(a) shows the typical RHEED pattern for the as-received Ge. Note the very faint rings centered on the primary beam which suggest the presence of polycrystalline material on the surface. After etching for one minute in CP4 etch, which was used 10 minutes after mixing, the pattern of Figure 61(b) was obtained. The enhancement of the Kikuchi lines indicates a higher degree of crystal perfection, however, some rings denoting the presence of polycrystalline material are also present.

Another Ge wafer was cleaned then etched two minutes in CP4. It was then mounted on the MBE substrate heater and exposed to simulate MBE growth conditions by: 1) pumping to UHV ($\sim 10^{-8}$ Torr range), 2) in the presence of As vapor, heating to 600 °C for five minutes (oxide removal) and then holding

(a) as received

(b) CP4 (one min.)

(c) CP4 (2 min; exposed to As_4 for 2 hr. at 500 °C)

(d) CP8 (2 min; exposed to As_4 for 2 hr. at 500 °C)

(e) modified Superoxol (8 min.)

Figure 61. RHEED Patterns for (111) Ge Substrates as a Function of Substrate Preparation.

at 500 °C for two hours. The RHEED pattern for this latter specimen is shown by Figure 61(c). The diffraction is very similar to that of Figure 61(b). In a related experiment a Ge wafer etched in CP8 for two minutes was selectively exposed to the Ga and As molecular beams for two hours at 500 °C. The RHEED pattern from the masked pattern of the specimen is given in Figure 61(d).

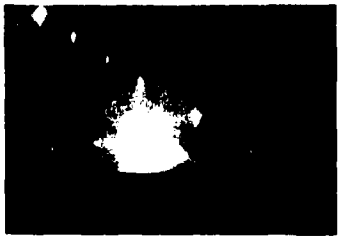
The modified Superoxol etch gave a good diffraction pattern with well defined Kikuchi lines and no ring pattern as illustrated by Figure 61(e). However, the surfaces of specimens etched with Superoxol were poor compared with those of other etchants.

Three Ge substrates were etched with CP8 for two minutes, each using solution that was 20 minutes old; these specimens were then used as substrates for MBE growth of GaAs on Ge. The growth rates were 1.0 $\mu m\ hr^{-1}$. Figure 62(a) shows the RHEED pattern for an epitaxial layer about 2 μm thick grown at a substrate temperature of 540 °C. Figure 62(b) shows the RHEED pattern for a similar layer grown at a substrate temperature of 500 °C. The RHEED pattern for the third layer grown at a substrate temperature of 460 °C is given in Figure 62(d). A fourth layer, B0908, 3.8 μm thick was grown at a temperature of 500 °C using a (111) Ge substrate that was cleaned in a dilute White etch for 20 minutes prior to growth. The RHEED pattern for this specimen is given in Figure 62(c). The White etch, when diluted with an equal part of DI water, gave good surfaces for etching times up to 20 minutes. No RHEED patterns were directly obtained for White-etched Ge wafers, however.

It is clear that the GaAs growth is primarily assuming the (111) orientation of the Ge substrate. The rings indicating partially polycrystalline

(a) A0825; T_{sub} = 540 °C

(b) A0828; T_{sub} = 500 °C



(c) B0908; T_{sub} = 500 °C

(d) A0829; T_{sub} = 460 °C

Figure 62. RHEED Patterns for 2.0 - 4.0 μm Thick Layers of GaAs Grown on (111) Ge Substrates for Various Substrate Temperatures.

material present in A0825, A0828, and A0829 are indexed as reflections from {220}, {422}, {440}, {642} and {660} planes. These are the dominant {hkl} reflections expected for (111) oriented diamond lattices. There are in addition a number of extra spots which appear to indicate twinning, particularly for growth at 540 °C (A0825). While a ring structure is not clearly evident in B0908, such structure could be masked by the reduced sharpness in the photographic plate.

A summary of the Ge etches investigated and the optical and RHEED characterization is given in Table 14.

A back reflection Laue X-ray was made for an as-received (111) Ge wafer. The incident radiation was a 20 keV beam from a Mo target. The Laue photograph given in Figure 63 shows the 3-fold symmetry of a (111) oriented substrate. The absence of spot elongation in the pattern is evidence of good single crystal structure. It is estimated that the weighted average of the sampling depth for this radiation is less than 50 μm. The Laue results suggest that the disordered regions observed in the RHEED studies are residual features arising perhaps from the mechanical and chemical surface preparation.

Table 14. Summary of Substrate Preparation and Features of Optical and Electron Diffraction Characterizations for (111) Ge Substrates and MBE GaAs on (111) Ge.

Sample	Substrate Preparation		Optical Surface Features	Electron Diffraction Data
	Etch	Time (min.)		
Ge	none	*	smooth, polishing marks	faint spots and rings
Ge	CP8	2	fish scale; 1-50 μm dia.	extra reflections, rings
Ge	CP4	1	polish marks not removed	rings
Ge	CP4	2	fish scale; 20-70 μm dia.	strong rings
Ge	White	5-20	smooth	*
Ge	Superoxol	8	haze, pits	Kikuchi lines,
MBE A0825	CP8	2	mounds, dense terraces	extra reflections, rings
MBE A0828	CP8	2	ripple, mounds, some terraces	extra reflections, faint rings
MBE A0829	CP8	2	ripple, mounds, 2-3 μm linear defects	extra reflections, rings
MBE B0908	White	20	ripple, mounds, terraces	extra reflections

Figure 63. Back Reflection Laue Photograph of (111) Ge Substrate.

9.0 FUTURE WORK

This study of MBE materials has identified several areas where further work is needed. The electrical properties and photoluminescence spectra of unintentionally doped (p-type) and lightly doped (n-type) MBE GaAs indicate that details of the incorporation of defects and impurities are poorly understood. The p^+-n hyperabrupt varactor demonstrates the potential of MBE in providing flexible, tight doping control. Further exploitation of this control in fabricating millimeter wave and optical sources is indicated. Molecular beam epitaxy also provides unique opportunities for masking which are applicable in the planar monolithic technology. The diagnostic and deposition capabilities available in MBE promise to make a significant contribution toward understanding the mechanisms which govern the electrical behavior at interfaces between GaAs and insulator/metals. It also appears that MBE offers significant advantages in growing semiconductor materials other than GaAs or $Al_{1-x}Ga_xAs$ such as InP, $GaAs_yP_{1-y}$, $In_{1-x}Ga_xAs$, or $In_{1-x}Ga_xAs_yP_{1-y}$. Relatively little work has been directed toward defining the deposition conditions, structural properties doping parameters and electrical characteristics for ternary and quaternary MBE layers, however.

It is believed that the unique features which characterize semiconductor growth by MBE will continue to impact on a fundamental technological problem area facing the Navy: namely, the improvement in performance and reliability of solid state millimeter devices for use in EW systems, high resolution radar, and covert and wideband communications.

APPENDIX I. COMPUTING DOPING CONCENTRATIONS WITH C(V) AND Q(V) DATA

To a first approximation, the equivalent circuit of a reverse-biased Schottky diode can be visualized as a capacitance C_p in parallel with a conductance G. Both elements are a function of the bias voltage. Using the well known relationship for transforming from a parallel to a series reactive circuit, the junction capacitance C_s can be written as[66]

$$C_s = C_p\ (1 + Q^{-2}) \qquad \text{(A1)}$$

where $Q = 2\pi f C_p G^{-1}$ and

f = r.f. measurement frequency.

The expressions which yield the doping concentration profile in terms of distance W and concentration N for a Schottky barrier diode are

$$W = \frac{\varepsilon A}{C_s} \quad \text{and} \qquad \text{(A2)}$$

$$N = \frac{C_s^{\,3}}{q\varepsilon A^2} \left(\frac{dC_s}{dV}\right)^{-1} \qquad \text{(A3)}$$

where q = electronic charge,

ε = semiconductor permittivity,

A = diode area, and

V = bias voltage

If equation (A1) is substituted into Equation (A3), a relationship can be obtained which is valid for non-uniform profiles in terms of the variables C_p and Q:

$$N = \frac{C_p^3 (Q^2 + 1)^3}{q\epsilon A^2 Q^3 \left(Q(Q^2+1) \frac{dC_p}{dV} - 2C_p \frac{dQ}{dV}\right)} \qquad \text{(A4)}$$

Completely analogous results have been derived by Wiley and Miller[153] who express Equations (A1), (A2), and (A4) above as a function of C_p and a phase angle ϕ between the applied r.f. voltage and the diode current. Laboratory measurements of low Q diodes indicate that the two element equivalent circuit model may form an inadequate basis for deriving profiles when the diode Q as defined above is less than a value of 7.0.

APPENDIX II. ANNEALING GaAs IN AN As MOLECULAR BEAM

The successful encapsulation and thermal anneal of GaAs specimens is a frequent requirement in device fabrication process sequences employing ion implantation. Furthermore, it is well known that the surfaces of III-V compounds experience dissociative evaporation when heated to high temperatures. A simple experiment was performed to test the possibility that surface dissociation of GaAs could be reduced by conducting the anneal in a flux of As molecules generated in the MBE sustem[154].

Three GaAs substrates with 001 surfaces were annealed in the MBE system for 15 minutes at temperatures of 720, 780, and 820 °C in an As atmosphere of 10^{-4}, 10^{-4}, and 5×10^{-5} Torr, respectively. These pressures were derived from a beam of As molecules aimed at the substrate. A portion of two of the substrates was shielded from a direct view of the As oven Micrographs of the surfaces after the high temperature anneal are shown in Figure 64. The surface texture under optical examination varied from a haze at the lowest temperature to metallic droplets covered with a thin crust in the 820 °C anneal.

A simple physical model is suggested in understanding these results. The Ga-rich segment of the binary GaAs liquidus indicates that As_2 is the primary species desorbing from the substrate at the anneal temperatures[8]. Arsenic leaving the exposed surface is replaced by the impinging flux of As_4 molecules from the arsenic oven. At high temperatures, the sticking coefficient of As_4 in the presence of a Ga surface population approaches a value of 0.5[155]. The heated Ta shield blocks direct As_4 bombardment while serving to confine As_2 over the underlying substrate. If the sticking coefficient of As_2 approaches unity in the presence of free Ga at high

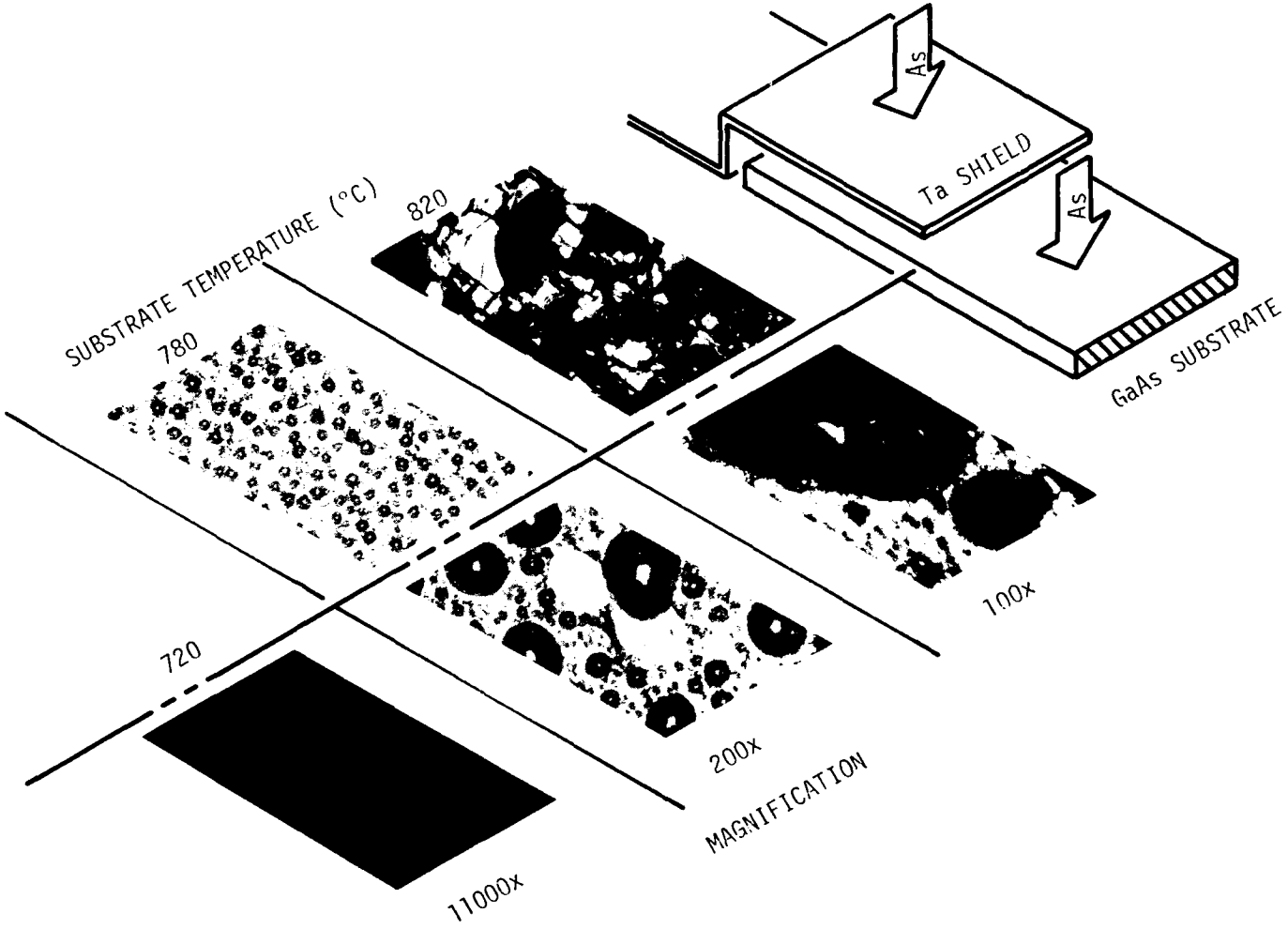


Figure 64: SEM and Optical Micrographs of the Surface Topography of Three GaAs Substrates After a High Temperature Anneal in an As Molecular Beam. Anneal Time in Each Case was 15 min.

temperatures, then the shield could be more effective in limiting the erro-sion of surface As_2. At 820 °C, the As_4 pressure was at least an order of magnitude below the equilibrium vapor pressure of As_2 while at 720 °C the reverse conditions holds. At 780 °C the two pressures were comparable in magnitude.

Although thermal anneals of GaAs at 850 °C have been reported using As sources, the quantity of As involved was substantial (40 mg of As for each cm^3 ampoule volume)[156]. The modification in surface topography observed in the present study indicates that an 800 °C anneal sequence cannot be easily achieved with convenient As_4 pressures. A greater potential exists for successfully annealing implants requiring lower temperature anneals in the 600 - 700 °C range.

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